

A Catalog-based AIG-Rewriting Approach to the Design of Approximate Components

Mario Barbareschi, Salvatore Barone, Nicola Mazzocca, and Alberto Moriconi

Abstract—As computational demand and energy efficiency of computer systems are becoming increasingly relevant requirements, traditional design paradigms are bound to become no longer appropriate, as they cannot guarantee significant improvements. The approximate-computing design paradigm has been introduced as a potential candidate to achieve better performances, by relaxing non-critical functional specifications. Anyway, several challenges need to be addressed in order to exploit its potential.

In this presentation, we propose a systematic and application-independent approximate design approach suitable to combinational logic circuits. Our approach is based on non-trivial local rewriting of and-inverter graphs (AIG), reducing the number of AIG-nodes and possibly resulting in lower hardware resources requirements. We adopt multi-objective optimization to carefully introduce approximation while aiming at optimal trade-offs between error and hardware-requirements. We evaluate our approach using different benchmarks, and, in order to measure actual gains, we perform actual synthesis of Pareto-optimal approximate configurations. Experimental results show that the proposed approach allows achieving significant savings, since resulting approximate circuits exhibit lower requirements and restrained error w.r.t. their exact counterparts.

Furthermore, because of architectural differences between FPGA and ASIC technologies, ASIC-tailored approximation techniques are usually unable to provide similar results when targeting FPGAs. We therefore conducted an extensive experimental campaign, aimed to empirically show that the approach is also able to provide good trade-offs between error and FPGA resources, for both generic logic and arithmetic circuits.

Index Terms—Automated Design Methodology, Approximate Computing, Multi-objective Optimization, Approximate Logic Synthesis, AIG Rewriting, FPGA Synthesis, Multi-objective Simulated Annealing, Approximate Logic Design, Low Area Approximate Circuits, Low Power Approximate Computing Circuits.



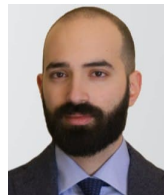
Mario Barbareschi received the PhD in Computer and Automation Engineering in 2015 and the Master Degree in Computer Engineering cum laude in 2012 both from the University of Naples Federico II. His research interests include Hardware Security and Trust, Cyber Physical Security, Approximate Computing and embedded systems design based on the FPGA technology. He has authored more than 60 peer-reviewed papers published in leading journals and international conferences.



Nicola Mazzocca is full professor of Computer Systems at the Department of Electrical Engineering and Information Technologies of the University of Naples Federico II. Since 1994, he has held numerous university courses and in professional training activities on different topics, including, high-performance systems, distributed systems, embedded systems, security, and reliability. His research activities concern: computer architecture, distributed systems, high-performance systems, and safety-critical applications. He is author of more than 250 papers on international journals, books, and conference proceedings of congresses.



Salvatore Barone received the PhD in Information Technologies and Electrical Engineering in 2022, and the Master Degree in Computer Engineering cum laude in 2018, both from the University of Naples Federico II, Italy. His research interests include Safety Critical Systems, Railway Systems, Approximate Computing and Embedded Systems based on the FPGA technology.



Alberto Moriconi received the Master Degree in Computer Engineering cum laude in 2019, from the University of Naples Federico II, Italy, where he is currently a PhD student. His research interests include Approximate Computing, Safety Critical Systems, Railway Systems, and Embedded Systems based on the FPGA technology.

- *Mario Barbareschi, Salvatore Barone, Nicola Mazzocca, and Alberto Moriconi are with the Department of Electrical Engineering and Information Technologies, University of Naples Federico II, Naples, Italy.
E-mail: [firstname.lastname@unina.it]
Authors are listed in alphabetical order.*

Manuscript received xxx, 2020