Dynamic partial reconfiguration on heterogeneous embedded platforms: timing predictability

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Introduction

- **Safety/Mission critical systems** look at **Heterogeneous Reconfigurable Computer Architectures** (HRCAs) as they enable
  - low SWaP (size, weight, and power) design solutions
  - high performance at acceptable power consumption
  - dependability

- HRCAs are **SoCs** containing microprocessors, dedicated accelerators, and one or more RCAs [1]
  - Xilinx/AMD Zynq7000, Zynq Ultrascale+, Versal
  - Altera/Intel Cyclone V SoC
  - Microsemi Fusion

References

[1] C. Insaurralde, "Reconfigurable computer architectures for dynamically adaptable avionics systems," in IEEE Aerospace and Electronic Systems Magazine, vol. 30, no. 9, pp. 46-53, Sept. 2015, doi: 10.1109/MAES.2015.140077.

Motivational examples involving HRCAs

Low SWaP – High Performance

- Robust real-time tracking on low-cost UAV platform [2]
  - Real-time automatic detection task acceleration using “microprocessor + FPGA” as HRCA
  - When necessary, the task is able to issue flight path changes to an UAV autopilot

Dependability

- Balancing High-Performance and safety in nanosatellites [3]
  - Trade-off performance and reliability at runtime using **Dynamic Partial Reconfiguration** on HRCA Zynq Ultrascale+
  - It considers configuration memory scrubbing and triple module redundancy

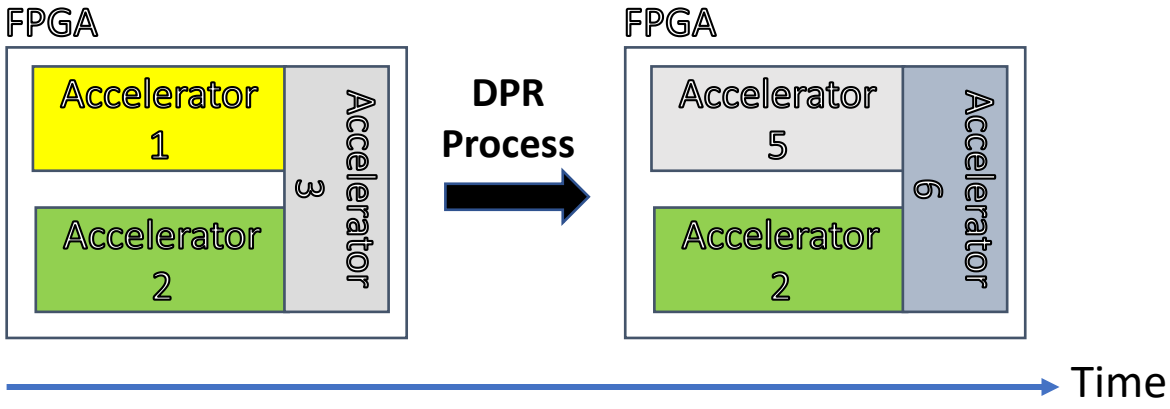
References

[2] G. Wigley and M. Jasiunas, "A low cost, high performance reconfigurable computing based unmanned aerial vehicle," 2006 IEEE Aerospace Conference, 2006, pp. 13 pp.-, doi: 10.1109/AERO.2006.1655800.

[3] Gantel, L.; Berthet, Q.; Amri, E.; Karlov, A.; Upegui, A. Fault-Tolerant FPGA-Based Nanosatellite Balancing High-Performance and Safety for Cryptography Application. *Electronics* 2021, *10*, 2148. https://doi.org/10.3390/electronics10172148

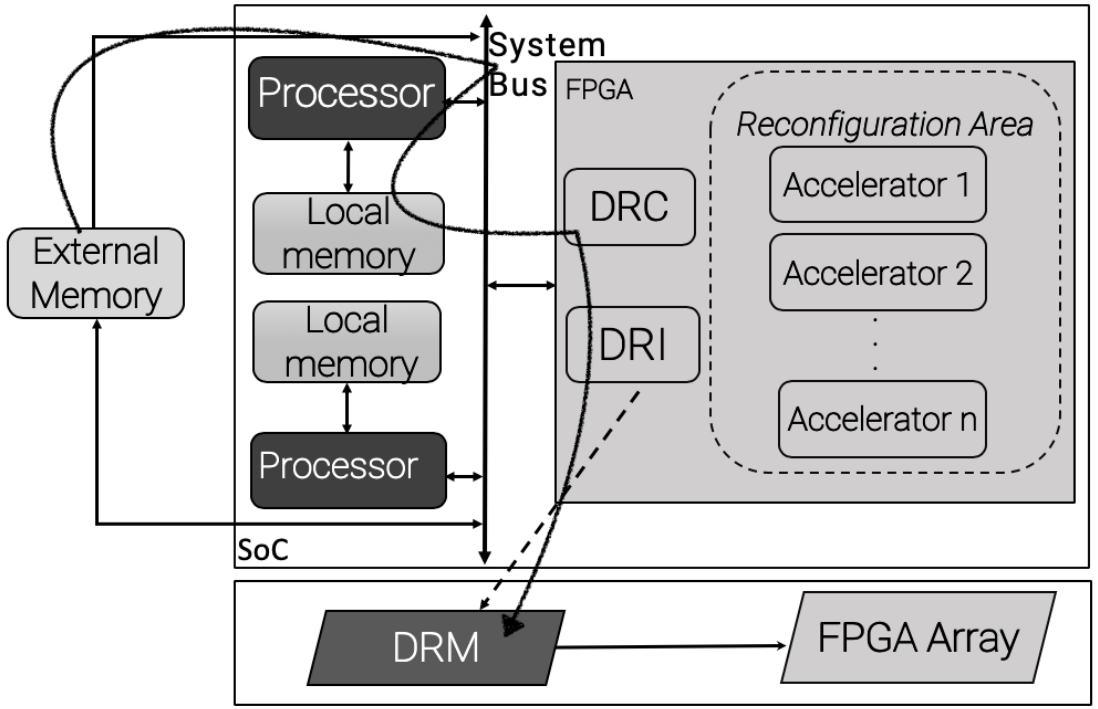
Dynamic Partial Reconfiguration on FPGAs

- **Modern HRCAs with FPGA allow DPR capabilities, enabling the user to reconfigure a portion of the FPGA dynamically (at runtime), while the remainder of the device continues to operate.**
  - DPR offers the possibility of virtualizing the FPGA area to support several hardware accelerators in time sharing
  - DPR offers the possibility to repair at runtime some areas of the SoC when faults happen



Reference platform for a DPR [4]

- The DPR is performed through a **reconfiguration path**
  - a processor transfers a reconfiguration file (bitstream, BS) from a shared external memory to a local memory;
  - the processor transfers the BS from local memory to **Dynamic Reconfiguration Memory** (DRM) through a **Dynamic Reconfiguration Controller** (DRC) and a **Dynamic Reconfiguration Interface** (DRI).
  - The DRM content directly acts on the FPGA array



References

[4] G. Valente, T. D. Mascio, L. Pomante and G. D'Andrea, "Dynamic Partial Reconfiguration Profitability for Real-Time Systems," in IEEE Embedded Systems Letters, vol. 13, no. 3, pp. 102-105, Sept. 2021, doi: 10.1109/LES.2020.3004302.

Research question and literature answers

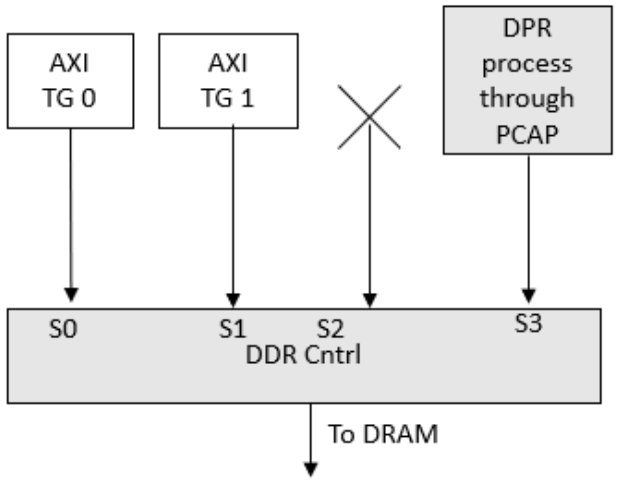
- **RQ: Is it possible to use DPR in safety/mission-critical systems while at the same time allowing an effective and efficient acceleration of tasks through the DPR itself?**

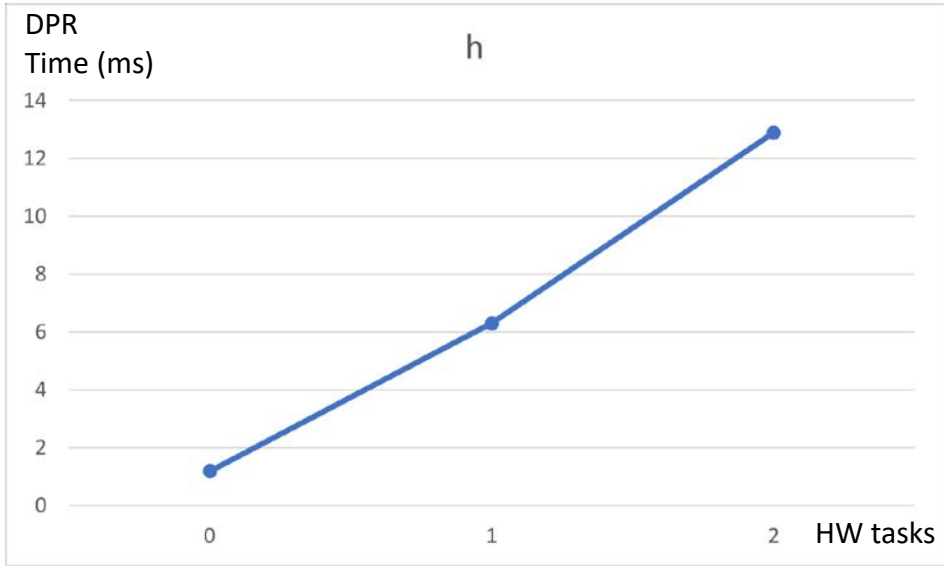
	DPR time	On-chip memory	System halting
[5]	✓	X	✓
[6]	X	✓	✓
[7]	✓	X	✓
[8]	✓	✓	X

- Gap
  - Some works assumes DPR time being only dependent on the reconfiguration interface
  - Some works assume to have dedicated memory for bitstream storage
  - Some works assume no other tasks executed during DPR

Example of DPR time variation on HRCA

- Target: Xilinx Zynq7000, 2 hardware tasks with BS 151 KB (4% of FPGA area), PCAP reconfiguration interface



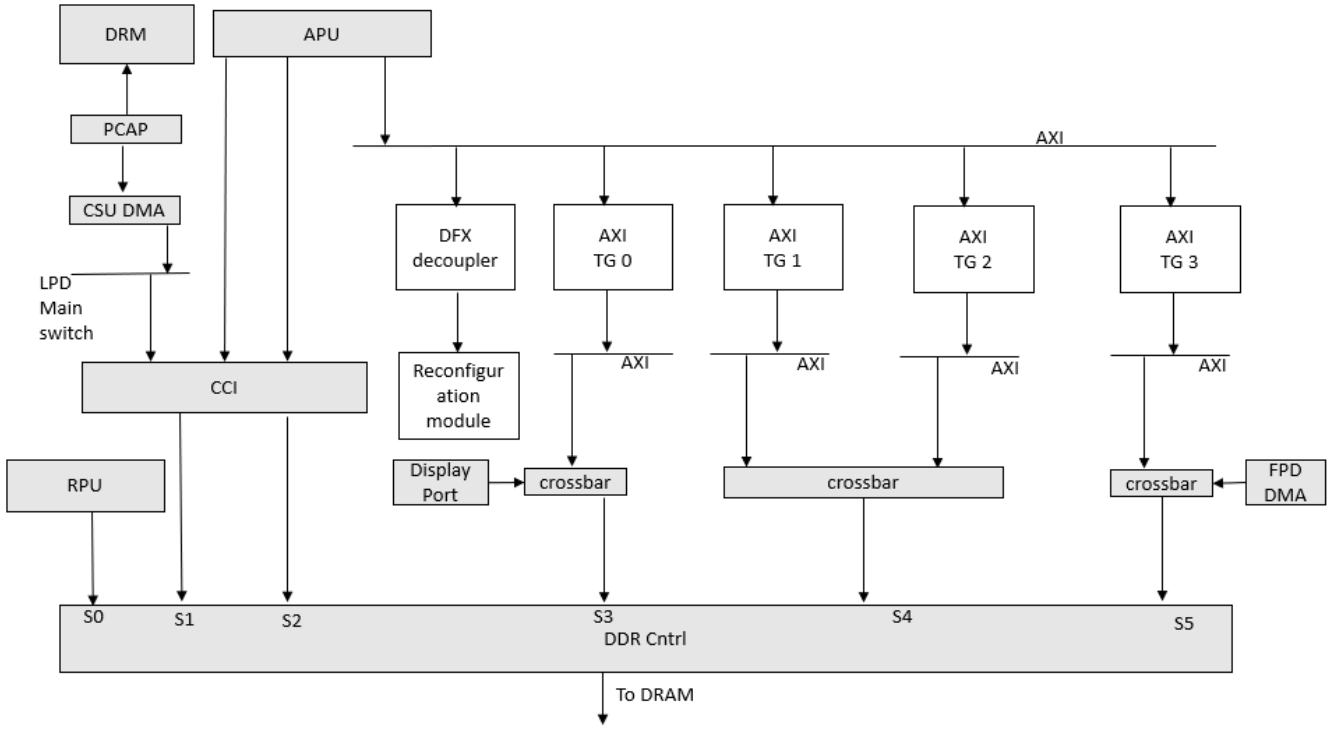


Requirements from certification

- No certification exists for the usage of HRCAs in the field of avionic
- EASA produced AMC 20-193
  - It recommends best practices to consider when dealing with MCPs, including considerations for dynamic allocation and multicore interference mitigation
  - From AMC 20-193
    - **MCP_Resource_Usage_3: identification of any interference cause by the use of shared memory, shared cache, an interconnect, or the use of any other shared resources, including shared I/O, and the verification of the means of mitigation chosen.**
- We build on that to extend the analysis recommended in AMC 20-193 to HRCAs

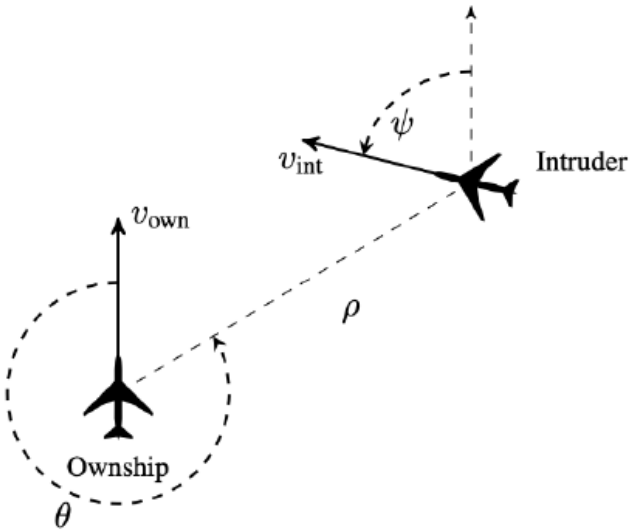
The proposed solution

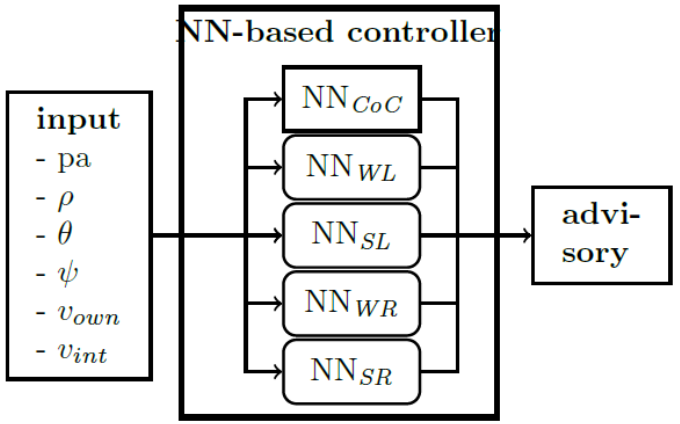
- Goal: to expose potential fault situations from other tasks in order to ensure appropriate levels of system functions availability
  - **Our solution: to develop tests to exercise each type of interference and to measure the impact of that interference on both task execution time and DPR time**
  - Target: Zynq Ultrascale+ ZU9EG SoC



Case study

- Recently, ACAS-X has been defined for next-generation airborne collision avoidance system
- **We consider a mixed-criticality task-set from ACAS-Xu (dedicated to UAV)**
  - System originally based on LUT used in real-time to solve conflicts
  - Neural network proposed to replace LUT [9]
  - Neural network workload and tasks executed on HRCA Zynq Ultrascale+





References

[9] M. Damour et al., "Towards Certification of a Reduced Footprint ACAS-Xu System: a Hybrid ML-based Solution," SAFECOMP 2021

Further References

- [5] M. Damschen, L. Bauer and J. Henkel, "CoRQ: Enabling Runtime Reconfiguration Under WCET Guarantees for Real-Time Systems," in IEEE Embedded Systems Letters, vol. 9, no. 3, pp. 77-80, Sept. 2017, doi: 10.1109/LES.2017.2714844.
- [6] A. Biondi, A. Balsini, M. Pagani, E. Rossi, M. Marinoni and G. Buttazzo, "A Framework for Supporting Real-Time Applications on Dynamic Reconfigurable FPGAs," 2016 IEEE Real-Time Systems Symposium (RTSS), 2016, pp. 1-12, doi: 10.1109/RTSS.2016.010.
- [7] L. Pezzarossa, M. Schoeberl and J. Sparsø, "A Controller for Dynamic Partial Reconfiguration in FPGA-Based Real-Time Systems," 2017 IEEE 20th International Symposium on Real-Time Distributed Computing (ISORC), 2017, pp. 92-100, doi: 10.1109/ISORC.2017.3.
- [8] Dörr, T., Sandmann, T., Schade, F., Bapp, F.K., Becker, J. (2019). Leveraging the Partial Reconfiguration Capability of FPGAs for Processor-Based Fail-Operational Systems. In: Hochberger, C., Nelson, B., Koch, A., Woods, R., Diniz, P. (eds) Applied Reconfigurable Computing. ARC 2019. Lecture Notes in Computer Science(), vol 11444. Springer, Cham. https://doi.org/10.1007/978-3-030-17227-5_8

Thank you!

Any questions?