UNIVERSITÀ di VERONA

Dipartimento di INFORMATICA

ESD Electronic Systems Design

Synthesis Verification Testing Power Communication

Methodologies for large-scale smart cyber-physical systems

Recent research of the Cyber-Physical Systems group of the University of Verona, department of Computer Science

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Graziano Pravadelli, Davide Quaglia, Tiziano Villa

Speaker: Nicola Bombieri

5th Italian Workshop on Embedded Systems, 2020, Catania

Outline

- Application context
- Design
  - Network synthesis
  - Embedded vision applications
- Modeling & Verification
  - Analysis of industrial plants
  - Joint system-network simulation
  - ROS-compliant containerized verification monitors
  - Catching sources of vulnerabilities
  - Automatic analog abstraction
  - Formal Methods for System Design
  - Run-time verification of parametric systems
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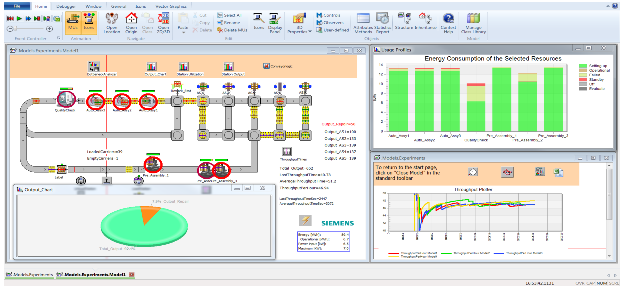
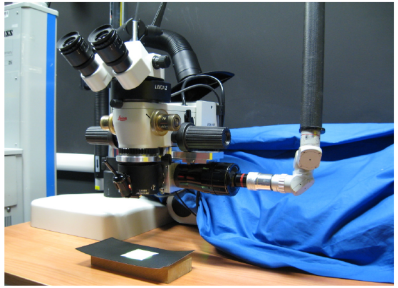
Large scale smart cyber-physical systems

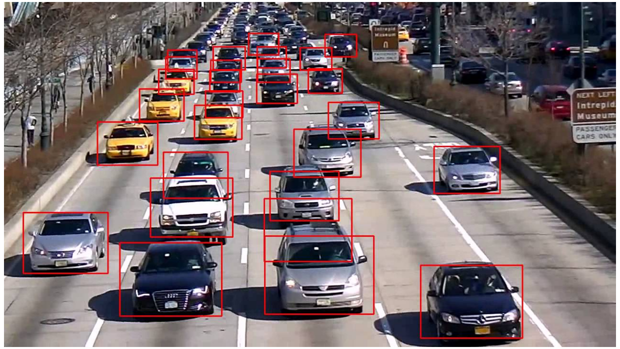
Industry 4.0



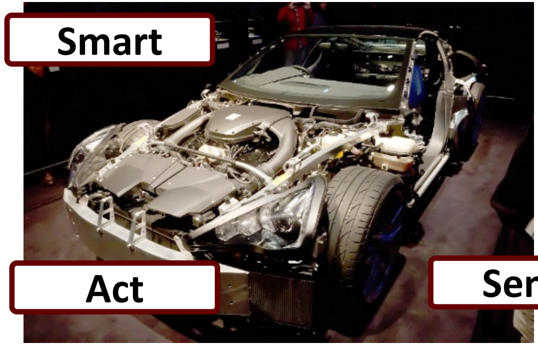
Robotic surgery



Embedded vision



Automotive



Smart

Act

Sense

Tight interaction between
- **processing,**
- **communication** and
- **sensing/actuation** devices

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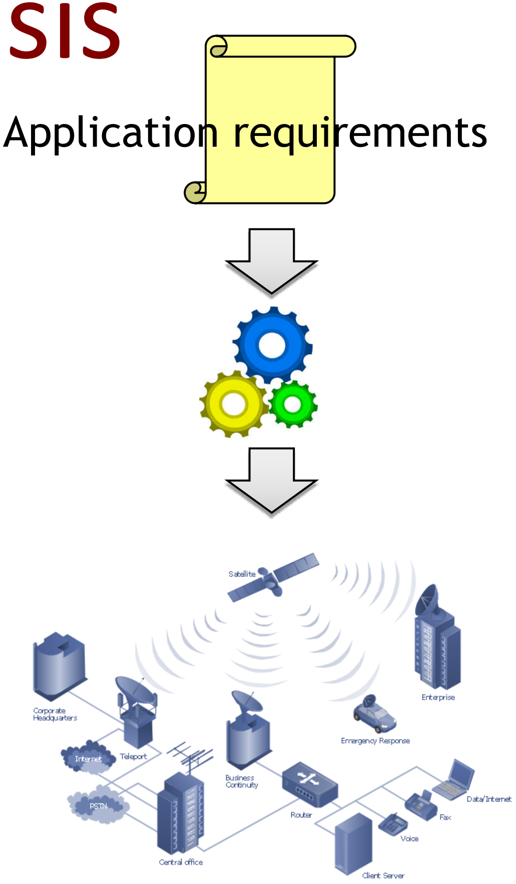
Davide Quaglia
Enrico Fraccaroli

Network Synthesis

- Automatic methodology to design the network infrastructure
  - Topology
  - Nodes (number, type)
  - Channel types
  - Protocols
- Optimal allocation of resources with respect to given metrics (e.g., cost, bandwidth, delay, robustness)
- Needed to address the challenging size and heterogeneity of future’s networks


Application requirements

Davide Quaglia
Enrico Fraccaroli

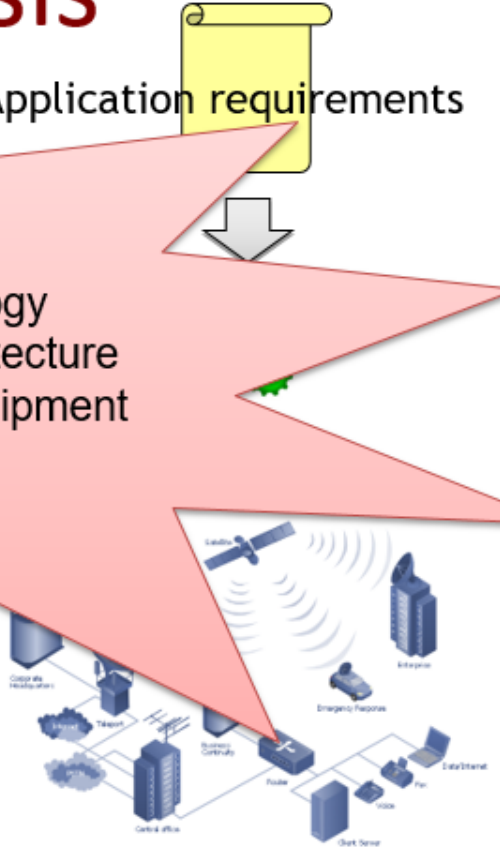
Network Synth sis

- Auto ethodology n the netw ct
  - Topolog
  -
  - Prot
- Opt respect to given bandwidth, del ust
- Needed to ad ess the ch ng size and heterogeneity of e's networks

Application to Industry 4.0

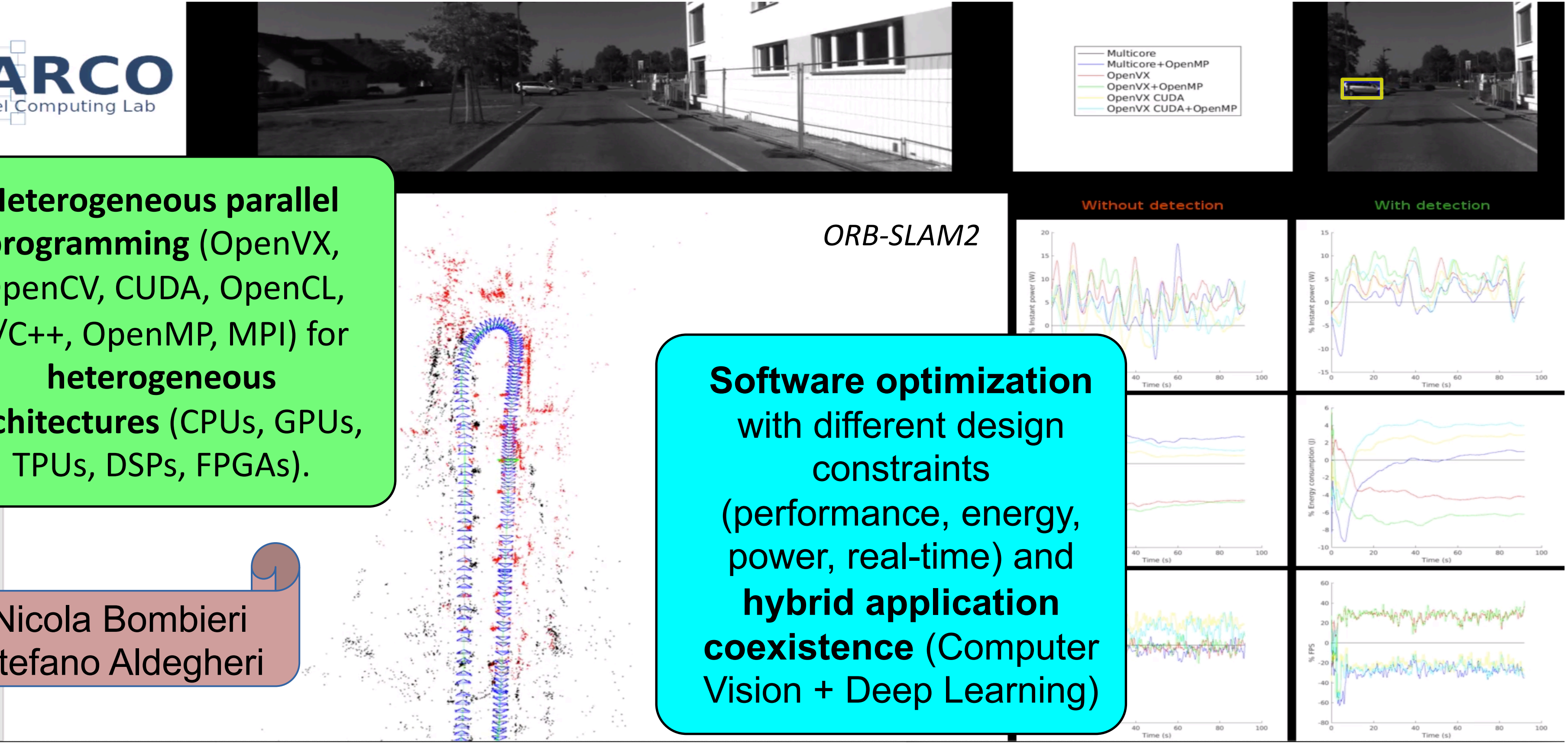
- Automatic design of the physical topology
- Automatic design of the OPC-UA architecture
- Automatic configuration of network equipment for cyber-security

Application requirements



Embedded vision applications

PARCO
Parallel Computing Lab



Heterogeneous parallel programming (OpenVX, OpenCV, CUDA, OpenCL, C/C++, OpenMP, MPI) for **heterogeneous architectures** (CPUs, GPUs, TPUs, DSPs, FPGAs).

Software optimization with different design constraints (performance, energy, power, real-time) and **hybrid application coexistence** (Computer Vision + Deep Learning)

Nicola Bombieri
Stefano Aldegheri

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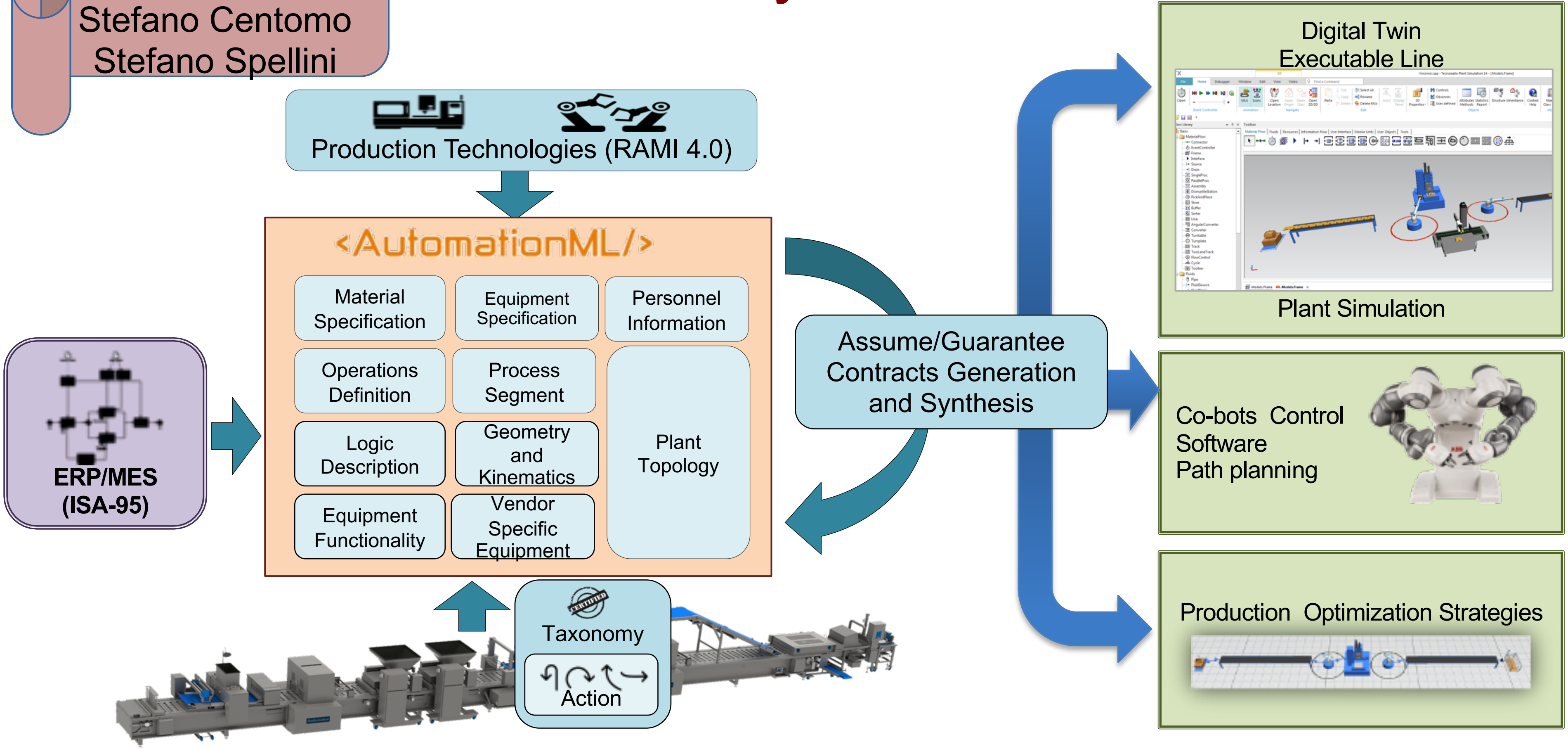
Formal Analysis of Industrial Plants

Franco Fummi
Stefano Centomo
Stefano Spellini



Production Technologies (RAMI 4.0)

<AutomationML/>

- Material Specification
- Equipment Specification
- Personnel Information
- Operations Definition
- Process Segment
- Plant Topology
- Logic Description
- Geometry and Kinematics
- Equipment Functionality
- Vendor Specific Equipment

ERP/MES (ISA-95)

Taxonomy

Action

Assume/Guarantee Contracts Generation and Synthesis

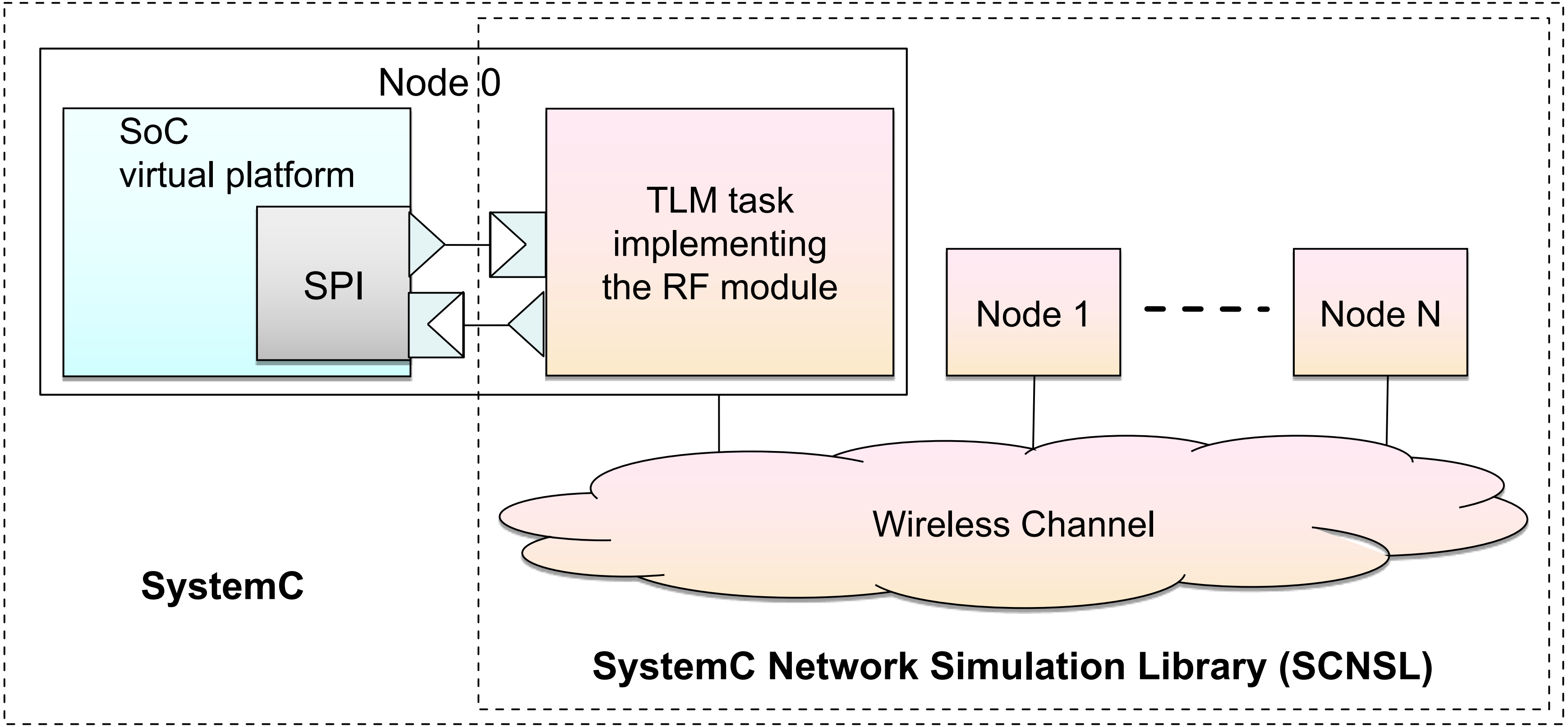
Digital Twin Executable Line

Plant Simulation

Co-bots Control Software
Path planning

Production Optimization Strategies

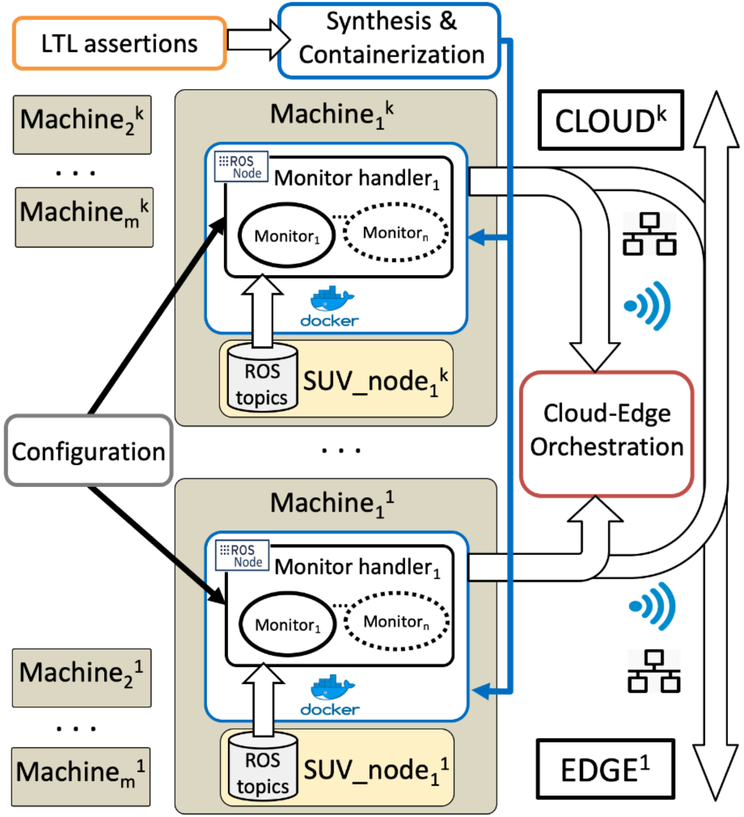
Joint System-Network Simulation



Graziano Pravadelli
Nicola Bombieri
Samuele Germiniani

ROS-compliant containerized verification monitors

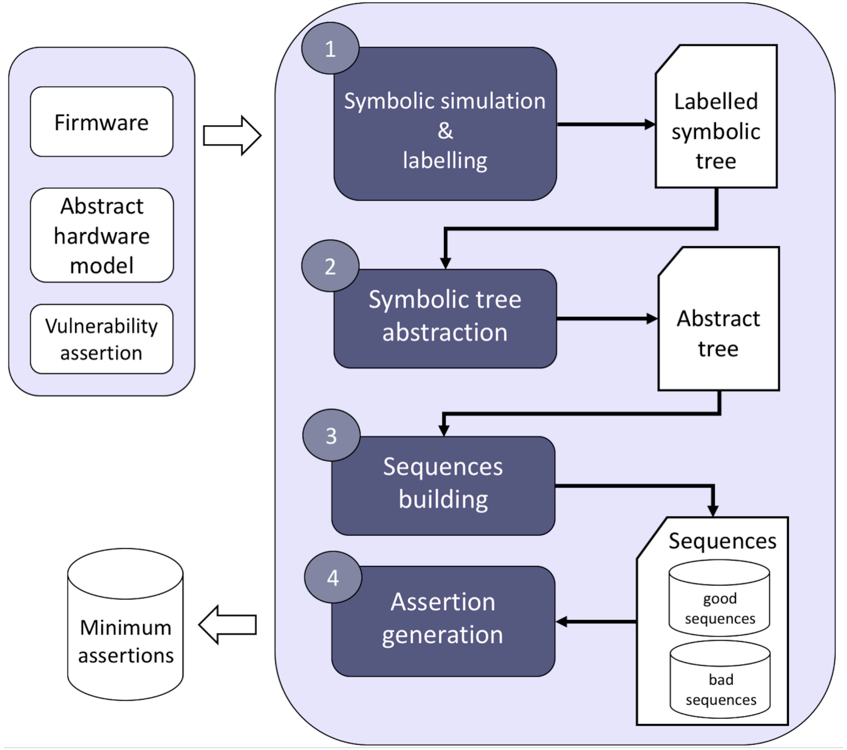
- Architecture and automatic flow to generate, orchestrate and deploy a ROS-compliant verification environment for robotic systems.
- Assertion-based verification through ROS-based monitors automatically synthesized from LTL assertions.
- Verification accuracy and real-time constraints addressed thorugh conteinerization across edge-server-cloud.



Graziano Pravadelli
Samuele Germiniani
Alessandro Danese

Catching sources of vulnerabilities

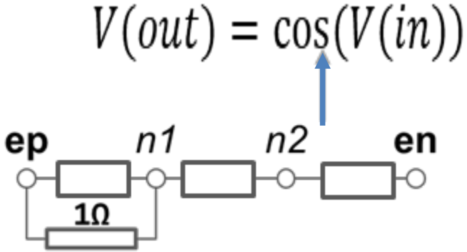
- Many tools for detecting vulnerabilities, but understanding the origin is more challenging
- Given an unwanted behavior, the proposed framework catches source of vulnerabilities
  - Through:
    - ✓ symbolic simulation and
    - ✓ sequence alignment
  - To generate:
    - ✓ assertions representing the minimum sequence of FW instructions that trigger the vulnerability



Automatic Analog Abstraction

Transform an analog design from **circuit level** to **functional level** and **move complexity** from **simulation** to **generation-time**

- *Functional* : **Mathematical** signal-flow description
- *Circuit* : Connection of **circuit** components



$$V(out) = \cos(V(in))$$

Methodology

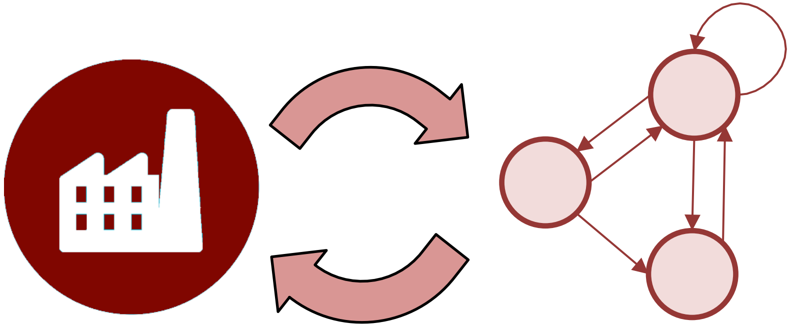
1. Parse circuit description
2. Apply Kirchhoff's laws
3. Reconstruct input-output relations of the model
4. Outlines the minimal set of equations for describing its behavior
5. Discretize and symbolicaly solves the minimal set of equations
6. Generate optimized C++ code

Tool: **HIFSuite**

Luca Geretti
Matteo Zavatteri
Davide Quaglia
Romeo Rizzi
Viktor Teren
Tiziano Villa

Formal Methods for System Design

with applications to Industry 4.0



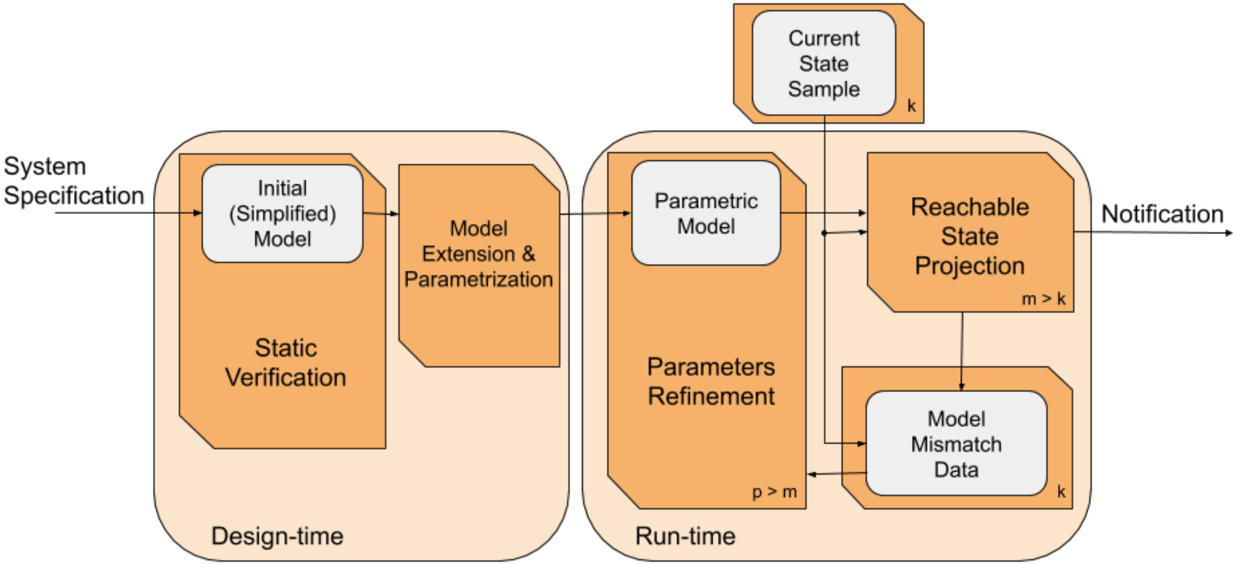
Activities:

- Application of formal methods to the industrial context and integration with edge/cloud techniques, with special reference to occupational safety
- Planning and scheduling under uncertainty: formal methods for temporal and resource controllability of industrial business processes
- Compositional and computational semantics for hybrid automata
- Characterization of quotient computation in discrete structures
- Decomposition of transition systems into Petri nets
- Logic synthesis

Luca Geretti
Tiziano Villa

Run-time Verification of Parametric Systems

- **Domain:** robotic and manufacturing systems
- **Problem**: identify potential unsafe behaviors of the real system during operation;
- **Approach**: from real states, evolve the model of the system in the future; periodically adapt the model to match the real states;
- **Methodology:** *parametric interval analysis* allows to model bounded uncertainties in the system;
- **Implementation**: in Ariadne with an additional ROS interface.



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