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An FPGA-Based Scalable Hardware Scheduler For Data-Flow Models

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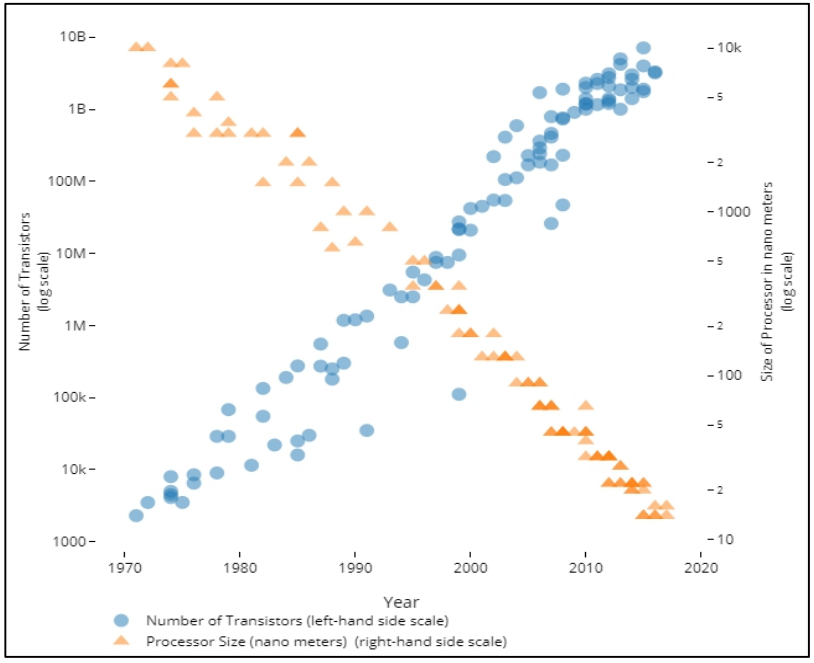
The end of Dennard scaling…

- Engineering community forced to find new solutions to improve performance with a limited power budget by [1]
  - ✓ Stop increasing clock frequency
  - ✓ Shifting to multicore processors

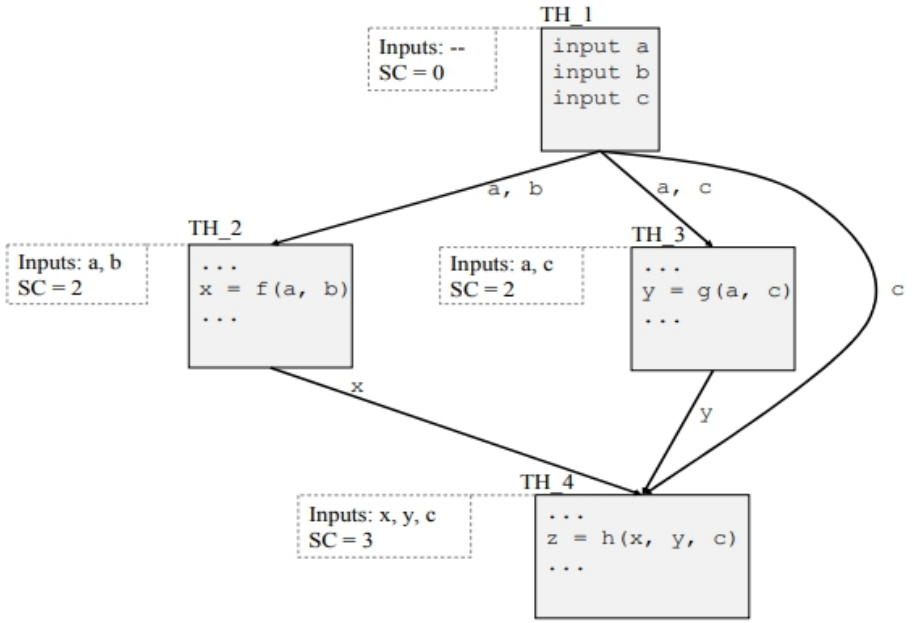


Moore's law 2018 – Source: Wikipedia

- Programming limitations to exploit full performance still remains…

The “DF-Threads” Data-Flow execution model

- The “DF-Threads” Data-Flow execution model is capable of taking advantage of the full parallelism offered by multicore systems[2][3][4][5][6][7]
  - ✓ Execution relies on data-dependencies
  - ✓ Parallel execution of data independent paths

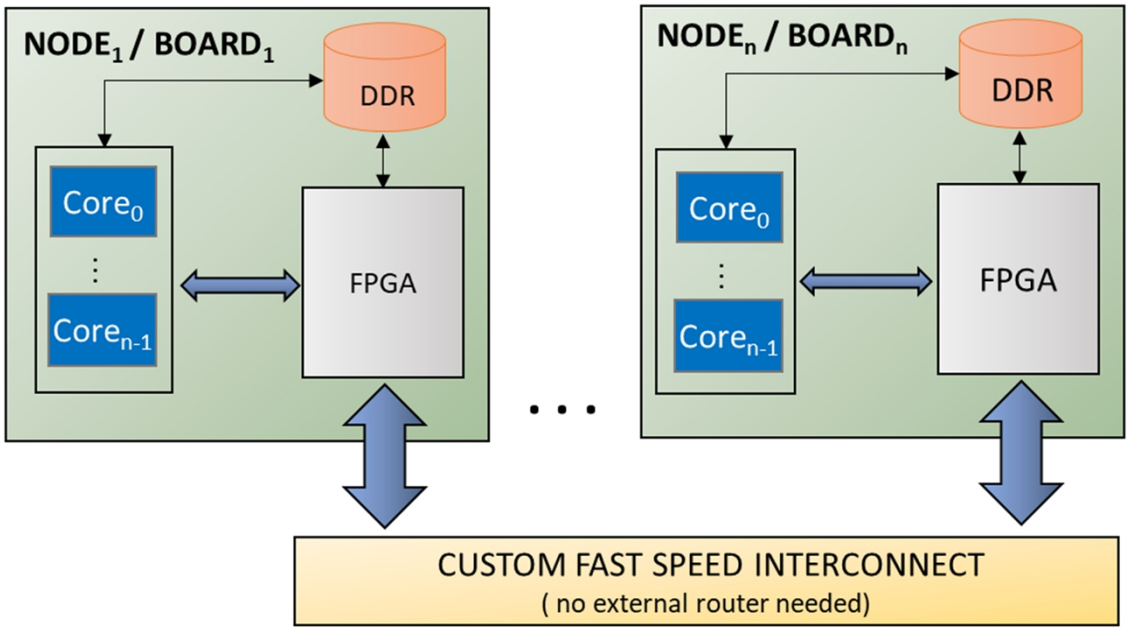


Hybrid Data-Flow Model

- DF-Threads based execution does not need to totally replace the conventional general purpose processors (GPP)
- Hybrid Model based on GPP and Field Programmable Gate Arrays (FPGA)
  - ✓ GPP cores are suitable for legacy or OS
  - ✓ FPGA can easily provide an efficient parallel execution via DF-Threads

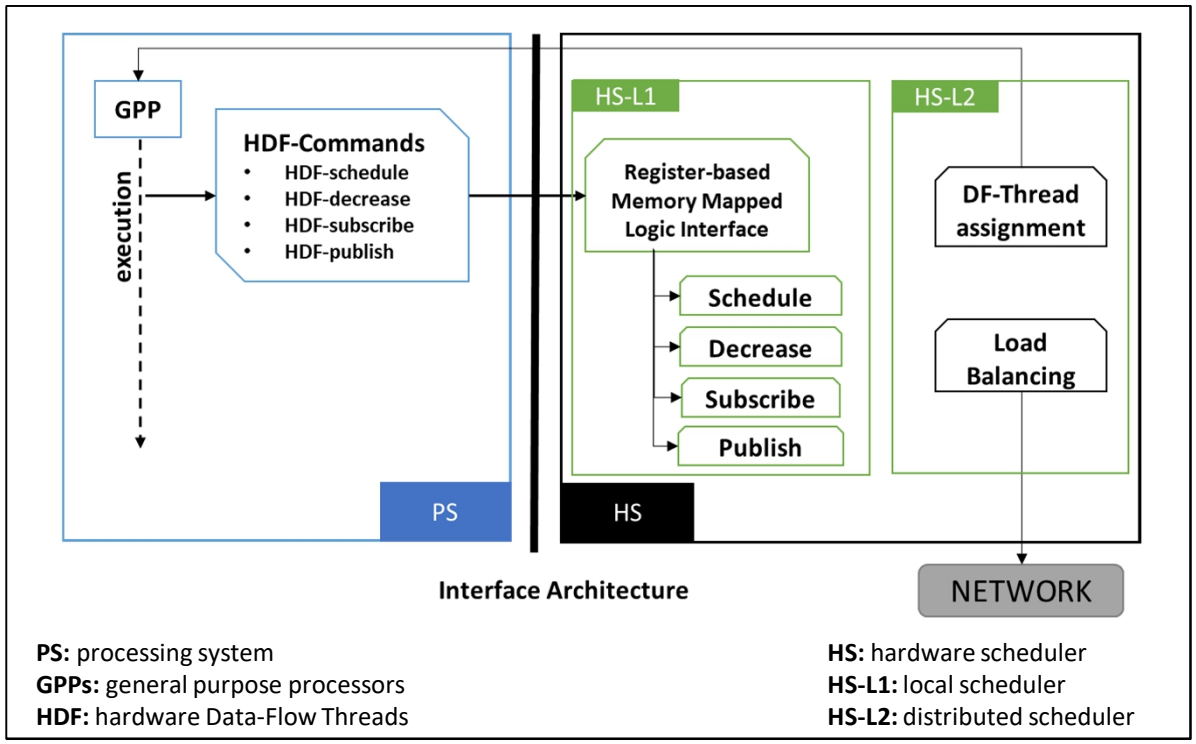
System Design

- A possible architecture to enable an easy distribution of the Data-Flow Threads (DF-Threads) among multiple core and multiple nodes [8]



The Idea

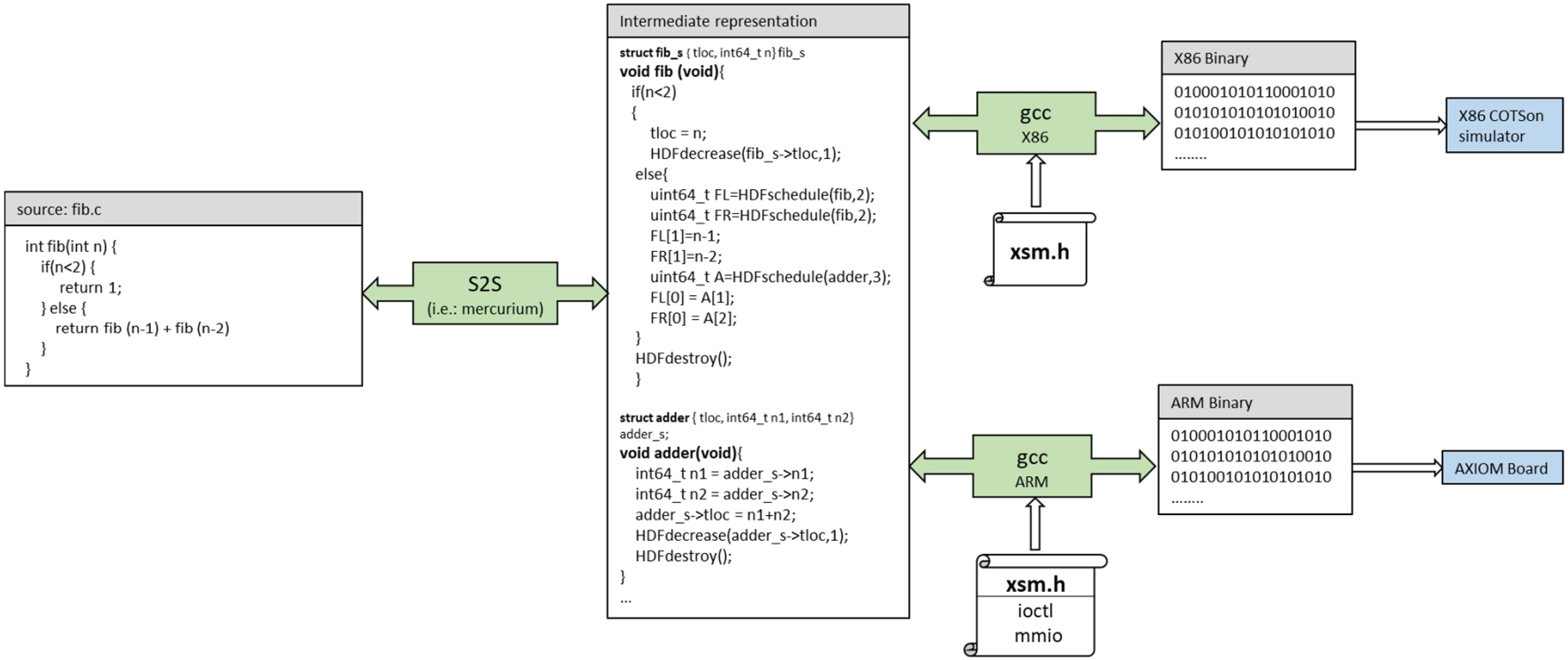
- Improving the execution of the Data-Flow Threads scheduling, by implementing an Hardware Scheduler (HS) on FPGA [9][10]



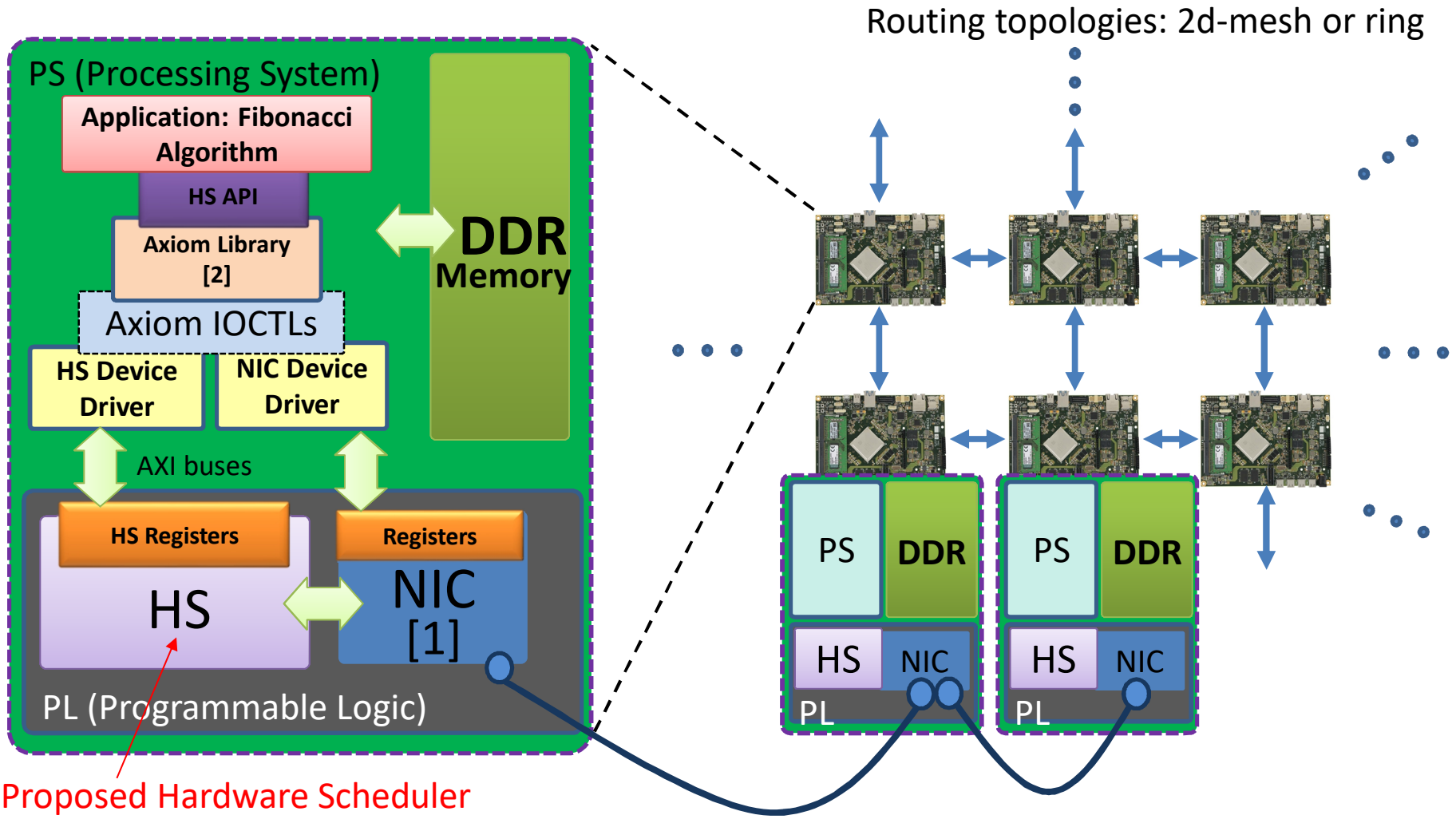
- The GPP:
  - ✓ Asynchronous APIs
  - ✓ Schedule DF-Threads
  - ✓ Execute DF-Threads
- The HS
  - ✓ Retrieves meta-information
  - ✓ Provides ready HDF-Threads
  - ✓ Distribute HDF-Threads on network

Compilation and testing flow

- Testing Environment
  - ✓ COTSon Simulator [11]
  - ✓ AXIOM Board [12]



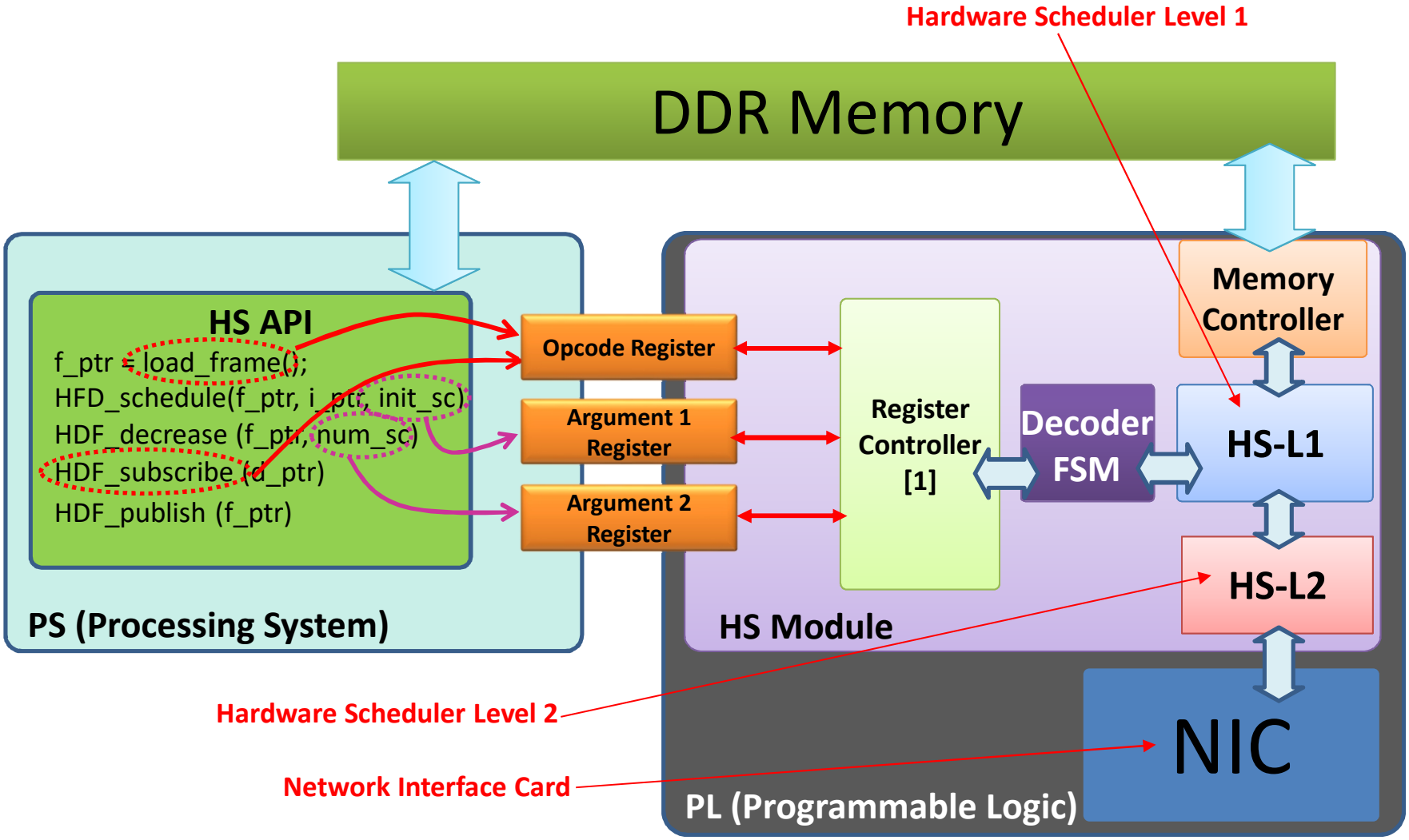
System Abstraction in a Perspective



[1] Vasileios Amourgianos-Lorentzos. “Efficient network interface design for low cost distributed systems” Master Thesis, 2017 at Technical University of Crete as part of the FORTH Axiom program.

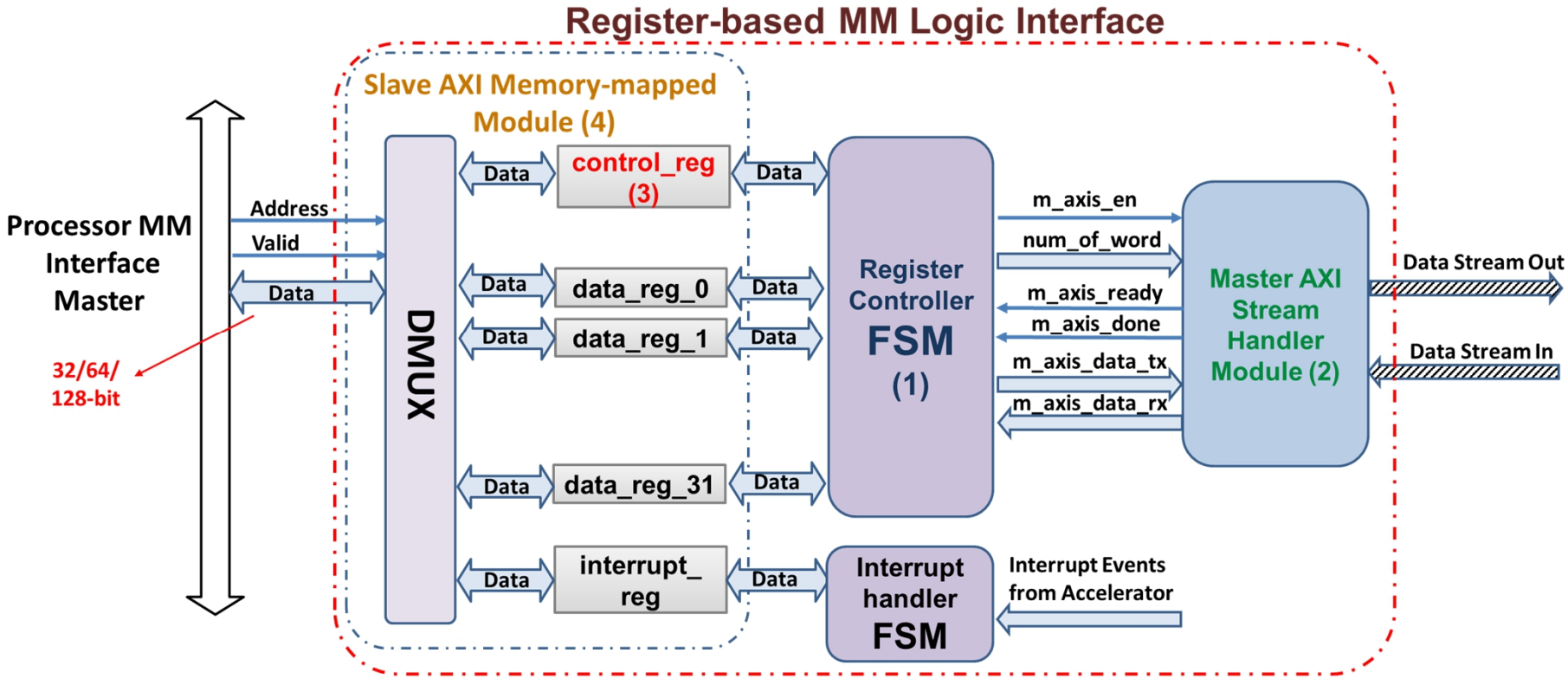
[2] Evidence Embedding Technology, 2017, “https://github.com/evidence

Hardware Scheduler (HS) Primitives



[1] F. Khalili, M. Procaccini and R. Giorgi. “Reconfigurable logic interface architecture for cpu-fpga accelerators.“ In HiPEAC ACACES-2018, pp. 1,4. Fiuggi, Italy, July 2018. Poster.

Register Controller [2]

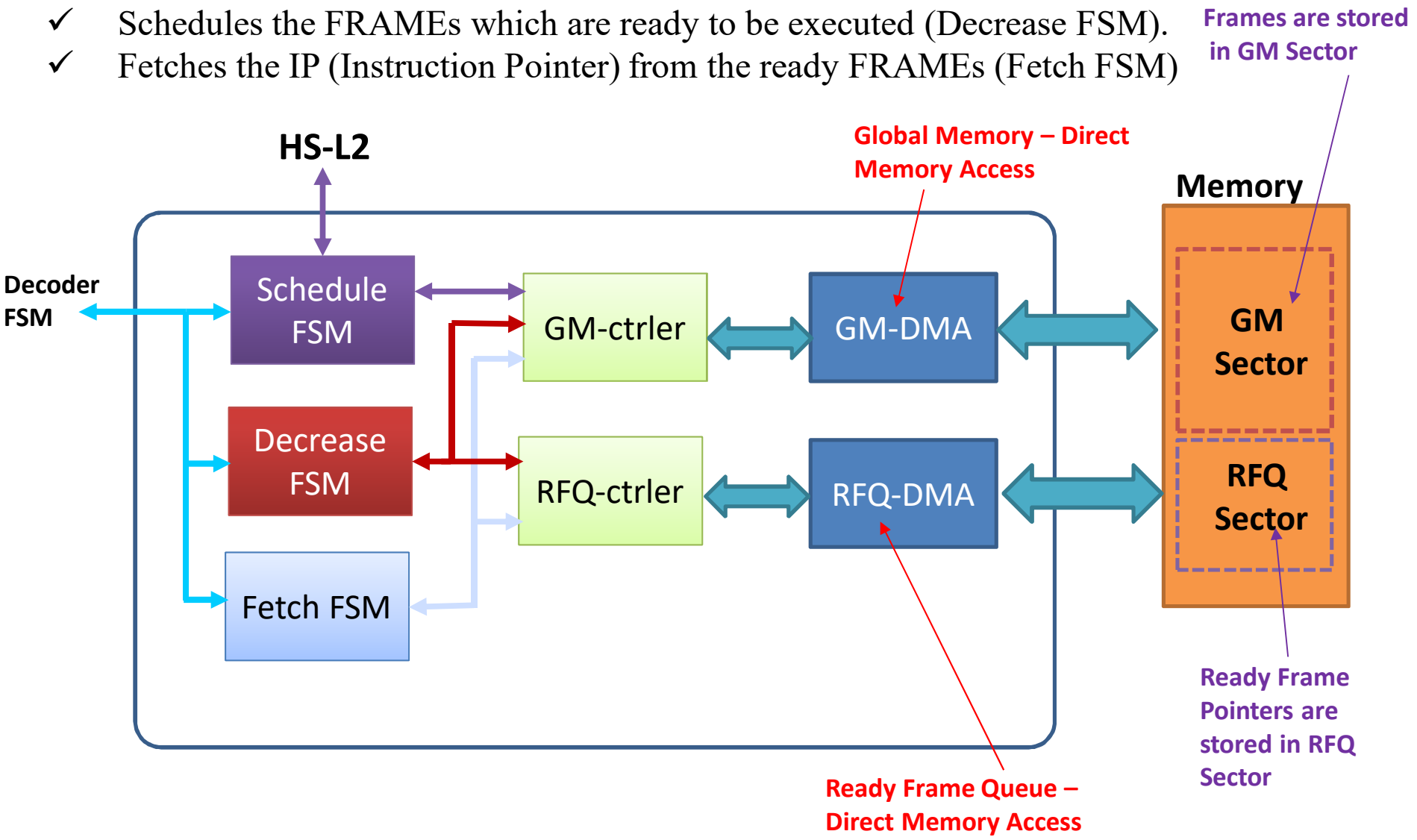


- ✓ The Write/Read access of each registers are separately controllable through the 'Control' register.
- ✓ The **Register Controller FSM (1)** is responsible to control **Master AXI Stream Handler Module (2)** and exchange data between AXI Stream and AXI memory mapped Domains.
- ✓ **Register Controller FSM (1)** also polls **control_reg (3)** and checks corresponding bit fields of each register if it is configured as write access or read access to set the direction of the data.

[2] F. Khalili, M. Procaccini and R. Giorgi. "Recongurable logic interface architecture for cpu-fpga accelerators." In HiPEAC ACACES-2018, pp. 1{4. Fiuggi, Italy, Julyy 2018. Poster.

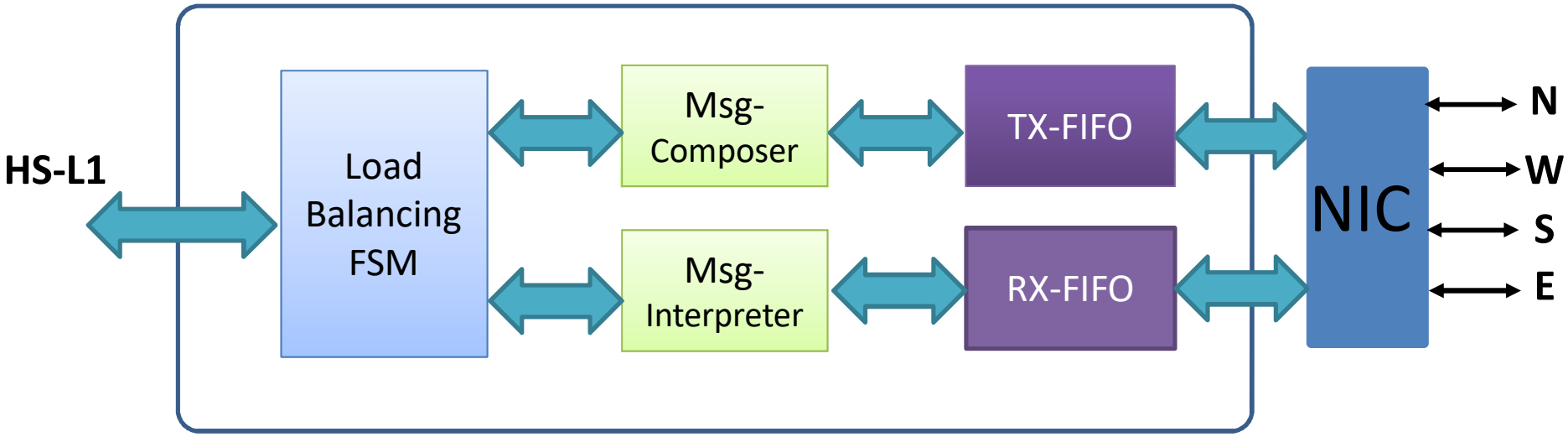
HS-L1 (Hardware Scheduler Level 1)

- ✓ Retrieves meta-information of FRAMEs (Schedule FSM)
- ✓ Schedules the FRAMEs which are ready to be executed (Decrease FSM).
- ✓ Fetches the IP (Instruction Pointer) from the ready FRAMEs (Fetch FSM)

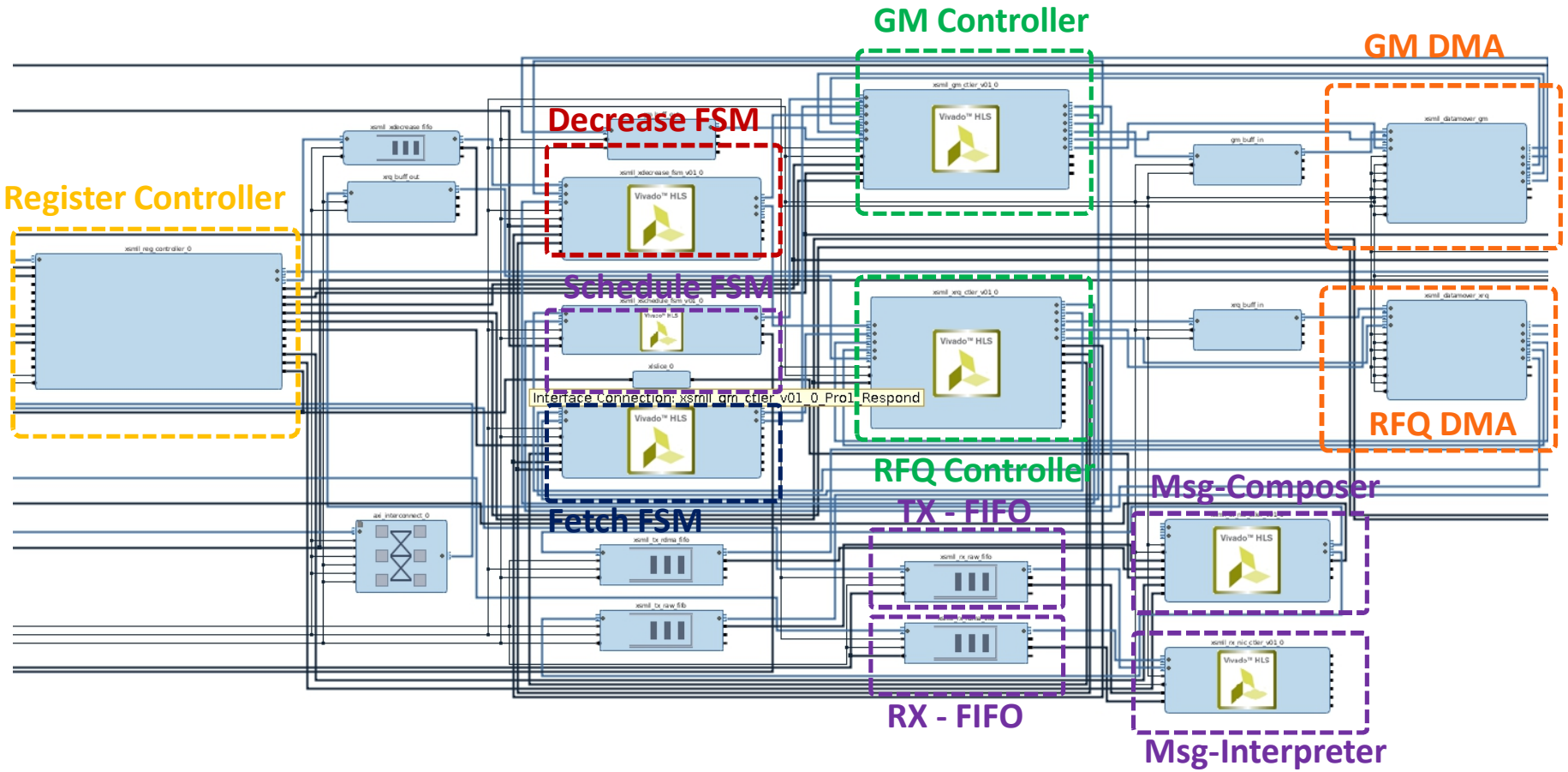


HS-L2 (Hardware Scheduler Level 2)

- ✓ Distribute FRAMEs in order to balance the loads throughout the network.
  - Work-stealing from remote nodes.
  - Off-load the works to remote nodes



Design Snippets



Evaluation – Execution Cycles

Operation	Data Width	Number Of Clock Cycles (PL).	
		Worst	Best
FIFO Enqueue/Dequeue	**64 bits**	**2**	**1**
Global Memory Write (DDR4)	16 bytes	48	40
Global Memory Read (DDR4)	16 bytes	38	38
Ready Queue Write	32 bits	48	40
Ready Queue Read	32 bits	44	44

Instruction Name	Delay Contributors	Number of Clock Cycles (PL).	
		Worst	**Best**
HDF-Schedule	*Total*	*49*	*40*
	DMA IP	48	39
	Decoder FSM	1	1
HDF-Decrease	*Total*	*89*	*43*
	DMA IP	86	40
	Decoder FSM	3	3
HDF-Fetch	*Total*	*85*	*34*
	DMA IP	*82*	*31*
	Fetch FSM	*3*	*3*

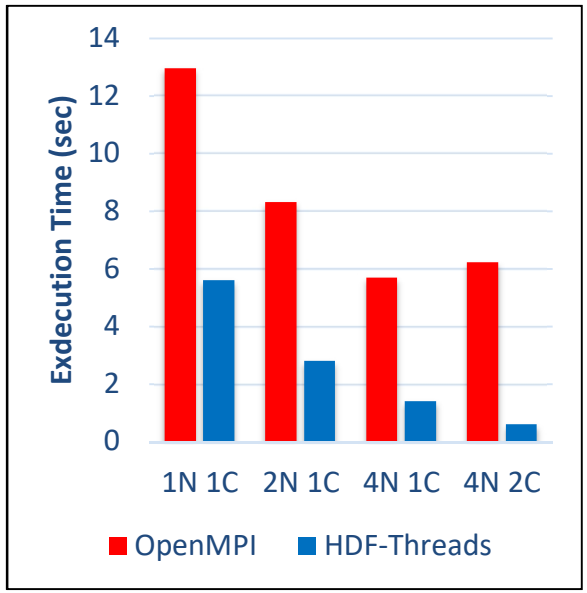
Evaluation – Resource Utilization

✓ Extracted resource utilization from Vivavo Design Suit 2016.4.
- Axiom board Zynq UltraScale+ XCZU9EG platform.

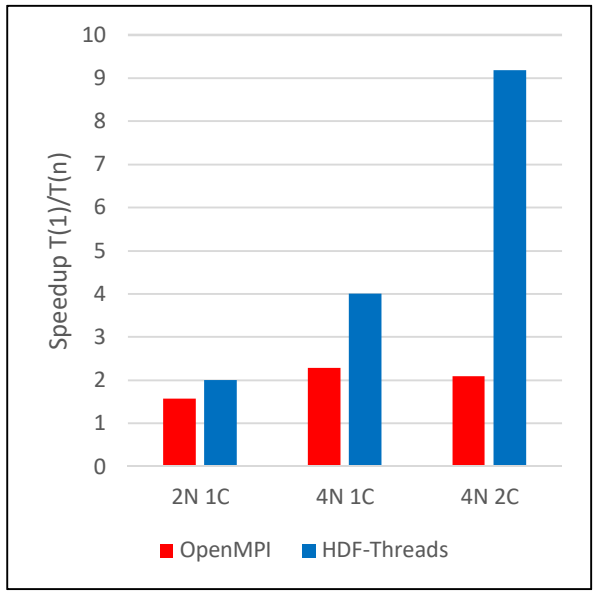
PL Units	Number of Units	Available	Utilization %
LUT	20357	274080	7.43
LUTRAM	2876	144000	2.00
FF	26116	548160	4.76
BRAM	49.50	912	5.43
IO	27	204	13.24
GT	2	16	12.50
BUFG	6	404	1.49

Results

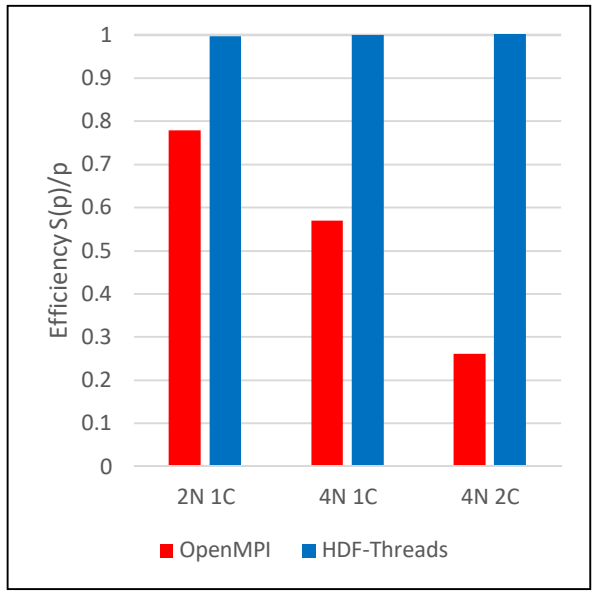
- HDF-Threads vs OpenMPI – Matrix Multiply Test 512+8



Execution Time



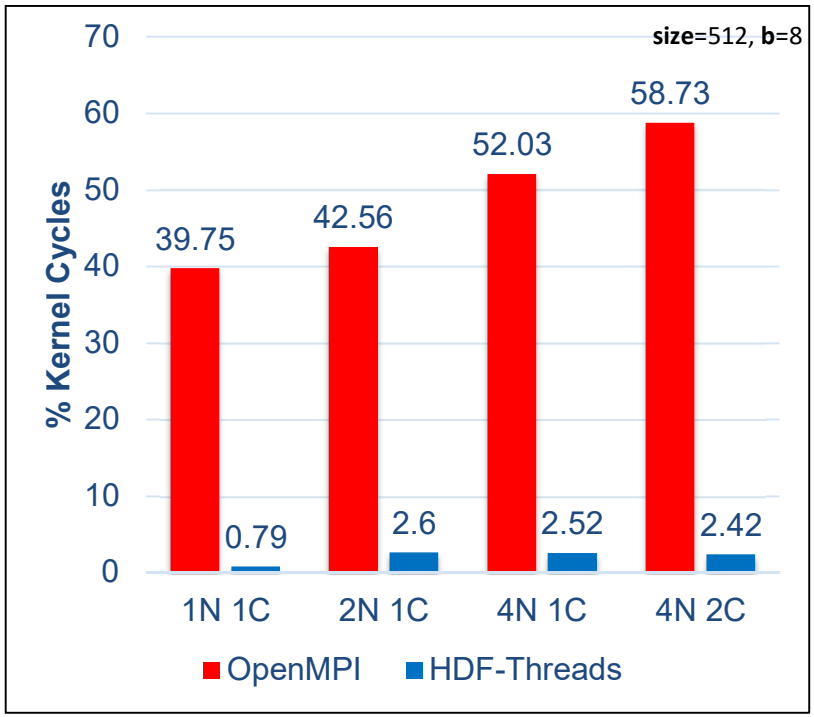
Speedup



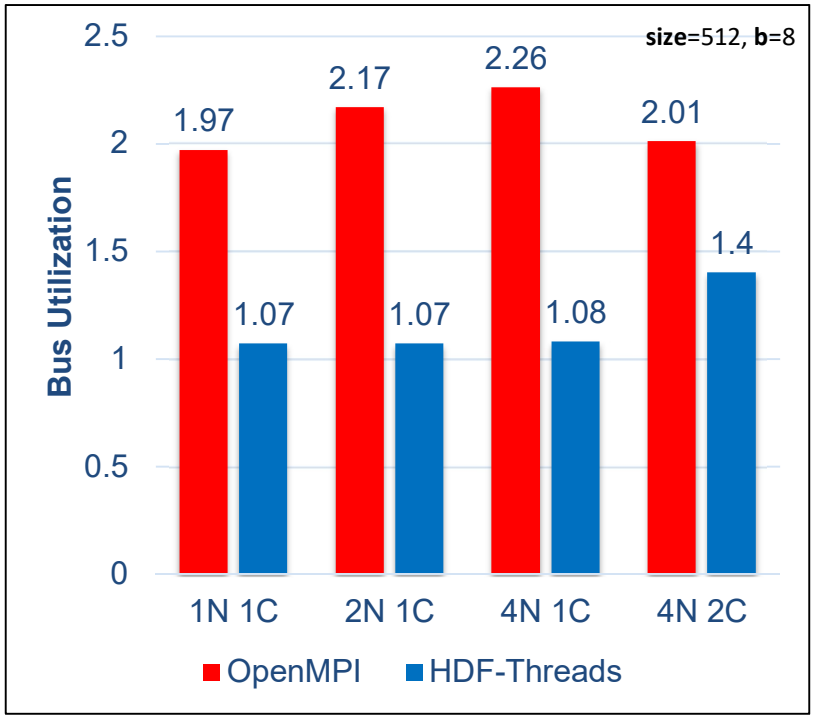
Efficiency

Results

- HDF-Threads vs OpenMPI – Matrix Multiply Test



Kernel Cycles



Bus Utilization

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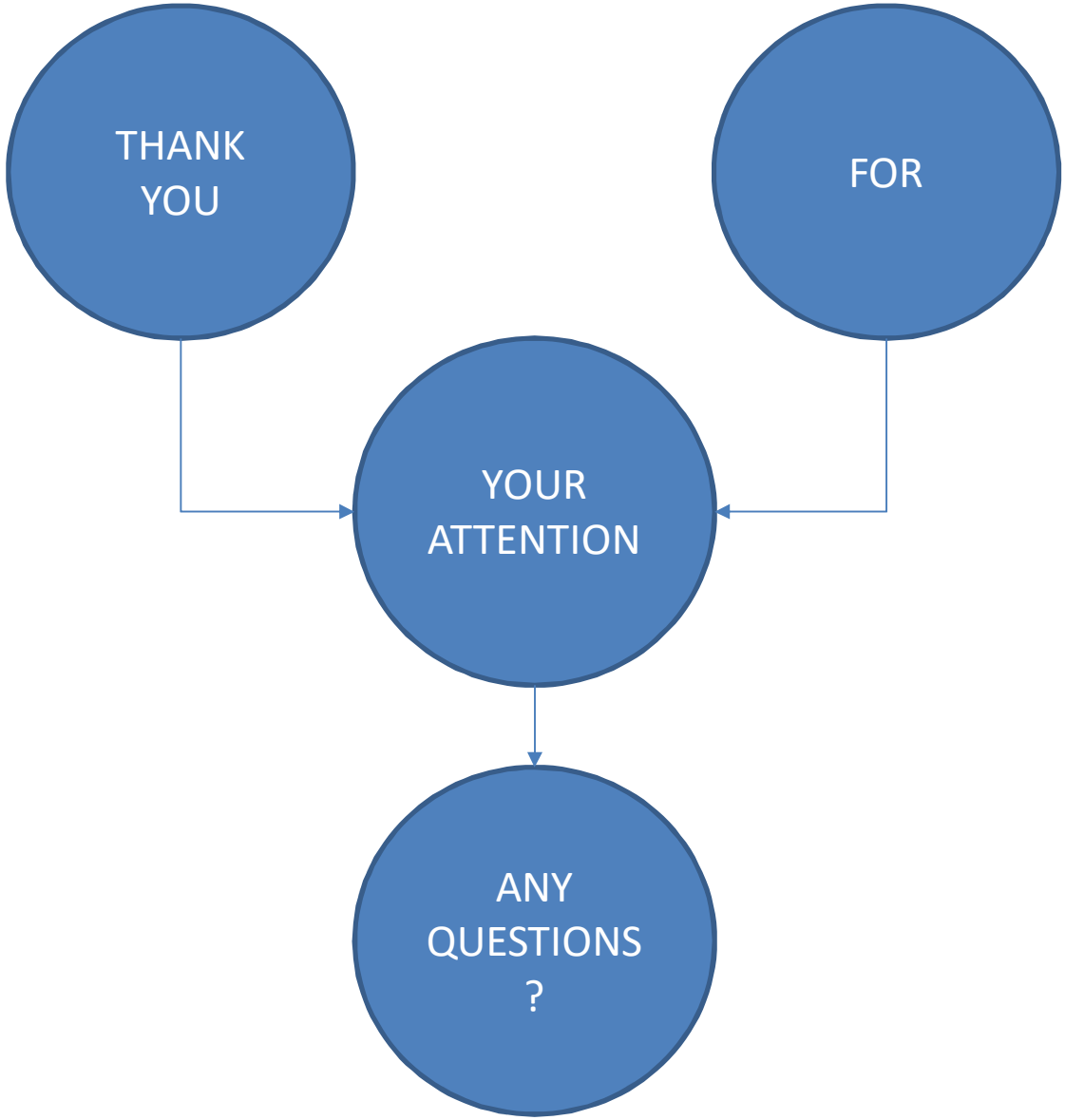
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