Logic synthesis techniques for switching nano-crossbar arrays

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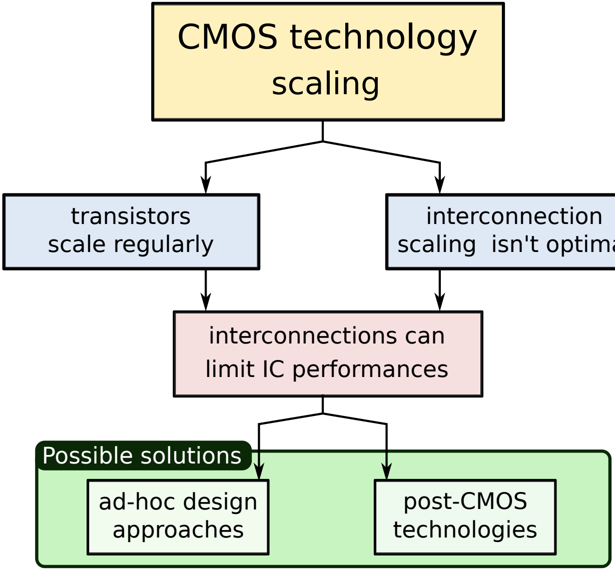
Problem and proposed solutions


CMOS technology scaling

transistors scale regularly

interconnection scaling isn't optimal

interconnections can limit IC performances

Possible solutions

ad-hoc design approaches

post-CMOS technologies

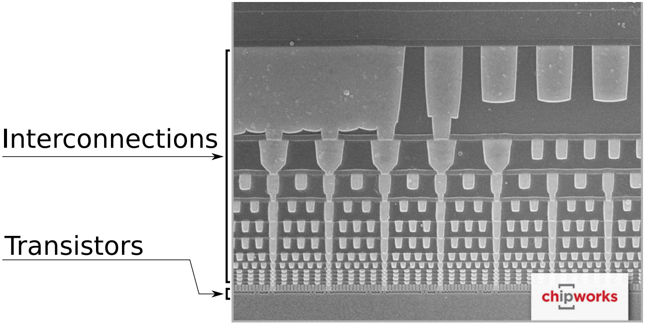
Interconnections in CMOS

Trend in Integrated Circuit industry:

- Improve throughput
- Reduce area
- Reduce power consumption

Technology scaling:

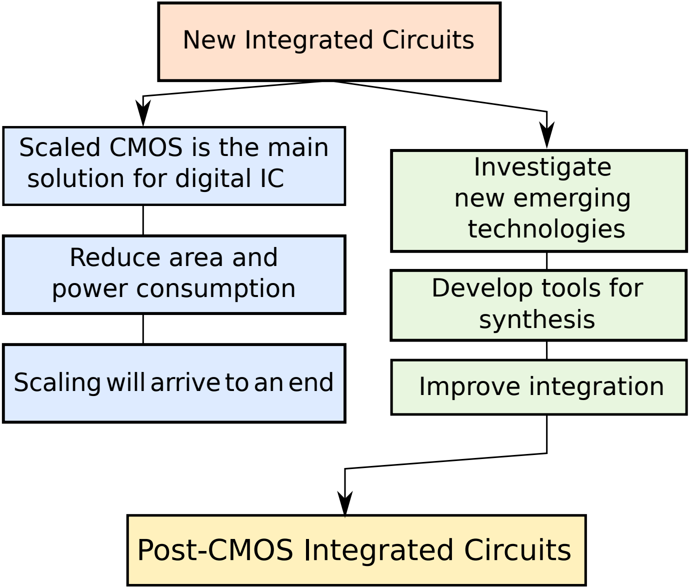
- Exploits the vertical dimension
- The number of metal layer increases
- Interconnections scaling isn't optimal



14 nm Intel – www.chipworks.com

New design approaches are needed

Emerging Technologies



New Integrated Circuits

Scaled CMOS is the main solution for digital IC

Reduce area and power consumption

Scaling will arrive to an end

Investigate new emerging technologies

Develop tools for synthesis

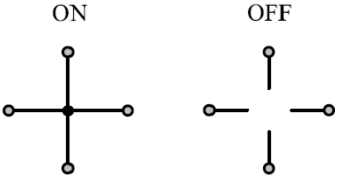
Improve integration

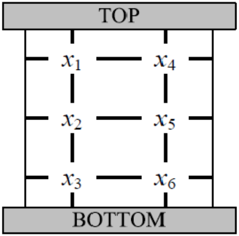
Post-CMOS Integrated Circuits

The Switching Lattices

Switching Lattices are **two-dimensional** array of **four-terminal** switches

- When switches are **ON** all terminals are connected, when **OFF** all terminals are disconnected
- Each switch is controlled by a boolean literal, **1** or **0**
- The boolean function f is the SOP of the literals along each path from **top** to **bottom**
- $f = x_1x_2x_3 + x_1x_2x_5x_6 +$ $+ x_4x_5x_2x_3 + x_4x_5x_6$





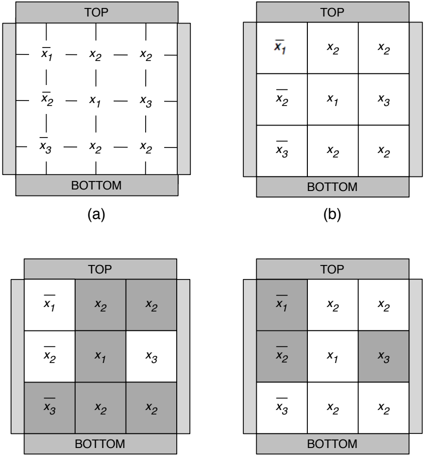
Switching Lattices

Switching Lattices:

- are two dimensional array of four-terminal switches
- emerging post-CMOS technology

A lattice output is:

- 1 if there is a connection between top and bottom
- 0 otherwise
- Gray cells are ON
- White cells are OFF
- a), b): the 4-terminal switching network and the lattice describing $f = \overline{x}_1\overline{x}_2\overline{x}_3 + x_1x_2 + x_2x_3$
- c), d): the lattice with input (1,1,0) and (0,0,1)



TOP
$\overline{x}_1$ x_2 x_2
$\overline{x}_2$ x_1 x_3
$\overline{x}_3$ x_2 x_2
BOTTOM
TOP
$\overline{x}_1$ x_2 x_2
$\overline{x}_2$ x_1 x_3
$\overline{x}_3$ x_2 x_2
BOTTOM
TOP
$\overline{x}_1$ x_2 x_2
$\overline{x}_2$ x_1 x_3
$\overline{x}_3$ x_2 x_2
BOTTOM
TOP
$\overline{x}_1$ x_2 x_2
$\overline{x}_2$ x_1 x_3
$\overline{x}_3$ x_2 x_2
BOTTOM

(a) (b)

(c) (d)

The synthesis methods

Altun-Riedel, 2012

- Synthesizes f and f^D from **top to bottom** and **left to right**
- It produces lattices with size growing **linearly** with the SOP
- Time **complexity is polynomial** in the number of products

TOP

LEFT

$\overline{x}_6$	$\overline{x}_8$	$\overline{x}_6$	x_4
$\overline{x}_8$	$\overline{x}_8$	$\overline{x}_5$	x_4
$\overline{x}_6$	$\overline{x}_7$	$\overline{x}_6$	x_4
$\overline{x}_7$	$\overline{x}_7$	$\overline{x}_5$	x_4
$\overline{x}_6$	$\overline{x}_5$	$\overline{x}_6$	x_4
x_1	x_1	x_1	x_1
$\overline{x}_2$	$\overline{x}_2$	$\overline{x}_2$	$\overline{x}_2$
x_3	x_3	x_3	x_3

RIGHT

BOTTOM

Gange-Søndergaard-Stuckey, 2014

- f is synthesized from **top to bottom**
- The synthesis problem is formulated as a **satisfiability problem**, then the problem is solved with a SAT solver
- The synthesis method searches for better implementations starting from an upper bound size
- The synthesis loses the possibility to generate both f and f^D

TOP

$\overline{x}_4$	x_6	x_7
x_2	x_5	x_8
$\overline{x}_1$	x_2	x_6
$\overline{x}_3$	0	$\overline{x}_6$

BOTTOM

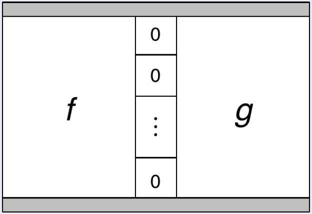
In both examples the synthesized function is:

$$f = \overline{x}_8\overline{x}_7\overline{x}_6x_3\overline{x}_2x_1 + \overline{x}_8\overline{x}_7\overline{x}_5x_3\overline{x}_2x_1 + x_4x_3\overline{x}_2x_1$$

Disjunction and conjunction of lattices

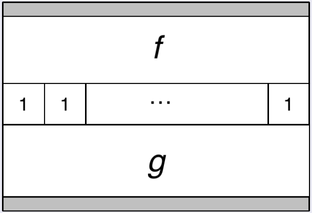
$f + g$

- separate the paths from top to bottom for f and g
- add a column of 0s
- add padding rows of 1s if lattices have different number of rows

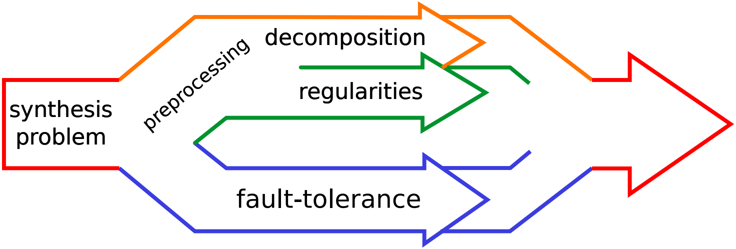


$f \cdot g$

- any top-bottom path of f is joined to any top-bottom path of g
- add a row of 1s
- add padding columns of 0s if lattices have different number of columns



Approach to the synthesis problem



Different approaches can be used to optimize lattice synthesis.
Common goals are:

- Produce optimal-size lattices
- Reduce synthesis time
- Find efficient methods for sub-optimal lattice synthesis

Use sub-optimal lattices when optimal synthesis requires too much computing time or memory

Preprocessing: decomposition example

$$z4(2) = x_3\overline{x}_4\overline{x}_6\overline{x}_7 + x_1\overline{x}_3x_4\overline{x}_6 + \overline{x}_1x_3\overline{x}_6\overline{x}_7 + \overline{x}_3\overline{x}_4x_6\overline{x}_7 + x_1x_3x_4x_6 + x_1\overline{x}_3\overline{x}_6x_7 + \overline{x}_1x_3\overline{x}_4\overline{x}_6 + \overline{x}_3x_4\overline{x}_6x_7 + \overline{x}_1\overline{x}_3\overline{x}_4x_6 + x_1x_3x_6x_7 + x_3x_4x_6x_7$$

The lattice size is 12×12

P-circuit representation:

$$P(z) = \overline{x}_1\, S(z^{=}) + x_1\, S(z^{\neq}) + S(z^{I})$$

$$S(z^{=}) = \overline{x}_3\overline{x}_4x_6 + x_3\overline{x}_4\overline{x}_6 + \overline{x}_3x_6\overline{x}_7 + \\ + x_3\overline{x}_6\overline{x}_7$$

$$S(z^{\neq}) = x_3x_4x_6 + \overline{x}_3x_4\overline{x}_6 + x_3x_6x_7 + \\ + \overline{x}_3\overline{x}_6x_7 + \overline{x}_3\overline{x}_4x_6\overline{x}_7 + x_3\overline{x}_4\overline{x}_6\overline{x}_7$$

$$S(z^{I}) = x_3x_4x_6x_7 + \overline{x}_3x_4\overline{x}_6x_7$$

$x_3x_4 \backslash x_6x_7$	00	01	11	10
00	0	0	1	1
01	0	1	0	1
11	1	0	1	0
10	1	1	0	0

$x_1 = 0$

$x_3x_4 \backslash x_6x_7$	00	01	11	10
00	0	1	0	1
01	1	1	0	0
11	0	0	1	1
10	1	0	1	0

$x_1 = 1$

$x_3x_4 \backslash x_6x_7$	00	01	11	10
00	0	0	1	1
01	0	0	0	1
11	1	0	0	0
10	1	1	0	0

$z^{=}$

$x_3x_4 \backslash x_6x_7$	00	01	11	10
00	0	1	0	1
01	1	1	0	0
11	0	0	1	1
10	1	0	1	0

$z^{\neq}$

$x_3x_4 \backslash x_6x_7$	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	0

z^{I}

$\overline{x}_1$	$\overline{x}_1$	$\overline{x}_1$	$\overline{x}_1$	0	x_1	x_1	x_1	x_1	x_1	x_1	0	x_4	x_4
x_6	x_3	x_6	x_3	0	x_6	$\overline{x}_3$	x_6	$\overline{x}_3$	$\overline{x}_3$	$\overline{x}_4$	0	x_7	x_7
$\overline{x}_3$	$\overline{x}_6$	$\overline{x}_3$	$\overline{x}_6$	0	x_3	$\overline{x}_6$	x_3	$\overline{x}_6$	$\overline{x}_4$	$\overline{x}_4$	0	x_6	$\overline{x}_3$
$\overline{x}_4$	$\overline{x}_4$	$\overline{x}_7$	$\overline{x}_7$	0	x_6	$\overline{x}_3$	x_6	$\overline{x}_3$	$\overline{x}_3$	$\overline{x}_7$	0	x_3	$\overline{x}_6$
1	1	1	1	0	x_3	$\overline{x}_6$	x_3	$\overline{x}_6$	$\overline{x}_7$	$\overline{x}_7$	0	1	1
1	1	1	1	0	x_3	x_4	x_3	x_7	x_6	x_3	0	1	1
1	1	1	1	0	x_4	x_4	x_7	x_7	$\overline{x}_3$	$\overline{x}_6$	0	1	1

Preprocessing: D-reducible function example

D-Reducible function

is a function that can be decomposed as:

$$f = \chi_A \cdot f_A$$

- χ_A is the characteristic function of an affine space A
- f_A is the projection of f onto A

$\overline{x}_4$	$\overline{x}_2$	$\overline{x}_2$	$\overline{x}_2$	$\overline{x}_2$	$\overline{x}_2$
x_2	$\overline{x}_5$	$\overline{x}_5$	x_4	$\overline{x}_5$	$\overline{x}_5$
$\overline{x}_3$	$\overline{x}_3$	$\overline{x}_3$	x_4	$\overline{x}_3$	x_4
x_5	$\overline{x}_2$	$\overline{x}_2$	x_2	$\overline{x}_2$	$\overline{x}_2$
$\overline{x}_4$	$\overline{x}_4$	$\overline{x}_4$	x_3	$\overline{x}_4$	x_3
x_1	x_1	x_1	x_1	x_1	x_1
x_{11}	x_{11}	$\overline{x}_7$	$\overline{x}_7$	$\overline{x}_7$	$\overline{x}_7$
x_9	x_9	$\overline{x}_7$	$\overline{x}_7$	$\overline{x}_7$	$\overline{x}_7$
x_{10}	x_{10}	$\overline{x}_7$	$\overline{x}_7$	$\overline{x}_7$	$\overline{x}_7$
x_8	x_8	x_8	x_8	x_8	x_8

x_3	$\overline{x}_3$	0
x_4	$\overline{x}_4$	0
x_1	x_1	0
x_8	x_8	0
1	1	1
x_3	$\overline{x}_5$	$\overline{x}_3$
$\overline{x}_2$	$\overline{x}_2$	x_2
x_{10}	1	x_5
x_{11}	$\overline{x}_7$	$\overline{x}_3$
x_9	$\overline{x}_7$	$\overline{x}_7$

$$\begin{aligned} f = \quad & x_1x_2\overline{x}_3\overline{x}_4x_5x_8x_9x_{10}x_{11} + x_2\overline{x}_2\overline{x}_3\overline{x}_4\overline{x}_5x_8x_9x_{10}x_{11} + x_1\overline{x}_2\overline{x}_3\overline{x}_4\overline{x}_5\overline{x}_7x_8 + \\ & + x_1\overline{x}_2x_3x_4\overline{x}_7x_8 + x_1\overline{x}_2\overline{x}_3\overline{x}_4\overline{x}_5\overline{x}_7x_8 + x_1\overline{x}_2x_3x_4\overline{x}_7x_8 \end{aligned}$$

$$f_A = \overline{x}_2x_3\overline{x}_7 + \overline{x}_2\overline{x}_5\overline{x}_7 + x_2\overline{x}_3x_5\overline{x}_6 + \overline{x}_2x_3x_9x_{10}x_{11} + x_2\overline{x}_3x_5x_9x_{10}x_{11}$$

$$\chi_A = x_1x_8(\overline{x_3 \oplus x_4})$$

Preprocessing: results

P-circuits

- **smaller lattices**: at least 24% of area reduction in 33% of functions
- **affordable computing time**, in a lot of cases find a solution in less time than the optimum one

D-reducible functions

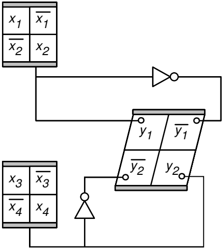
- **smaller lattices**: at least 24% of area reduction in 15% of functions
- **reduction of computing time** by 50% to find a solution than the optimum one

Example on regularities: autosymmetric boolean functions

Autosymmetric functions

- Let V be a vector subspace of $(\{0,1\}^n, \oplus)$. The set $A = \boldsymbol{\alpha} \oplus V$, $\boldsymbol{\alpha} \in \{0,1\}^n$, is an *affine space* over V with *translation point* $\boldsymbol{\alpha}$.
- $V = \boldsymbol{\alpha} \oplus A$, with $\boldsymbol{\alpha}$ any point in A.

x_1	$\overline{x_1}$	0	x_1	$\overline{x_1}$
$\overline{x_2}$	x_2	0	x_2	$\overline{x_2}$
1	1	0	1	1
x_3	$\overline{x_3}$	0	x_3	$\overline{x_3}$
x_4	$\overline{x_4}$	0	$\overline{x_4}$	x_4



- $f(x_1, x_2, x_3, x_4) = x_1 \oplus x_2 \oplus x_3 \oplus x_4$.
- decomposing: $f = g(y_1, y_2) = y_1 \oplus y_2$, where $y_1 = x_1 \oplus x_2$ and $y_2 = x_3 \oplus x_4$
- Multi-lattice: the sum of the areas of the lattices is smaller than the area of the optimum single-lattice

Autosymmetric functions decomposition results

Autosymmetric functions decomposition

- **smaller lattices**: at least 53% of area reduction in 48% of functions
- **affordable computing time**: in some cases is possible to find a solution in less time than the optimum one
- Some decomposed functions have **smaller total area** w.r.t. the lattice size in optimum case.

Drawbacks:

- Routing complexity increases
- It is necessary to add some inverters

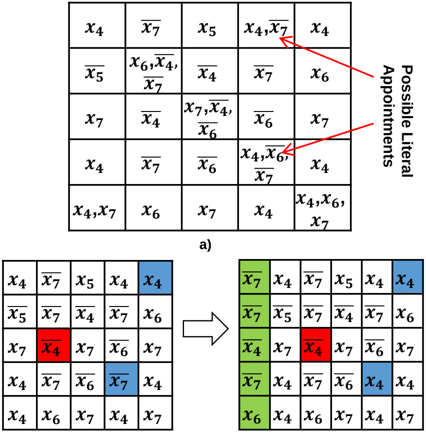
Switching Lattices and Defect Tolerance

- The switching lattices are made of self assembled systems
- The probability to have a defect on a single cell is up to 10%

- We consider stuck-at-one and stuck-at-zero fault
- Different synthesis methods produce lattices with different sensitivity to faults
- Current work aims at **developing a synthesis method that can improve defect tolerance**

Given Logic Function

$$f = x_4\overline{x_5}x_7 + \overline{x_4}x_6\overline{x_7} + \overline{x_4}\,x_5\overline{x_6}x_7 + x_4\overline{x_6}\,\overline{x_7} + x_4x_6x_7$$



x_4	$\overline{x_7}$	x_5	$x_4,\overline{x_7}$	x_4
$\overline{x_5}$	$x_6,\overline{x_4},$ $\overline{x_7}$	$\overline{x_4}$	$\overline{x_7}$	x_6
x_7	$\overline{x_4}$	$x_7,\overline{x_4},$ $\overline{x_6}$	$\overline{x_6}$	x_7
x_4	$\overline{x_7}$	$\overline{x_6}$	$x_4,\overline{x_6},$ $\overline{x_7}$	x_4
x_4,x_7	x_6	x_7	x_4	$x_4,x_6,$ x_7

Possible Literal Appointments

a)

x_4	$\overline{x_7}$	x_5	x_4	x_4
$\overline{x_5}$	$\overline{x_7}$	$\overline{x_4}$	$\overline{x_7}$	x_6
x_7	$\overline{x_4}$	x_7	$\overline{x_6}$	x_7
x_4	$\overline{x_7}$	$\overline{x_6}$	$\overline{x_7}$	x_4
x_4	x_6	x_7	x_4	x_7

b)

$\overline{x_7}$	x_4	$\overline{x_7}$	x_5	x_4	x_4
$\overline{x_7}$	$\overline{x_5}$	$\overline{x_7}$	$\overline{x_4}$	$\overline{x_7}$	x_6
$\overline{x_4}$	x_7	$\overline{x_4}$	x_7	$\overline{x_6}$	x_7
$\overline{x_7}$	x_4	$\overline{x_7}$	$\overline{x_6}$	x_4	x_4
x_6	x_4	x_6	x_7	x_4	x_7

c)

Conclusions

- Using **Boolean function preprocessing** we found some techniques to **reduce synthesis time and area occupation** of switching lattices:
  - In many cases decomposition leads to smaller lattices w.r.t. sub-optimal Altun synthesis solution
  - Preprocessing can reduce computing time generating sub-optimal lattices
  - In the case of autosymmetric functions the sum of the areas of the synthesized lattices can be smaller than the area of the optimal single-lattice solution

- We found some preliminary techniques to reduce lattice sensitivity to faults
- In future we will work on lattice defectivity analysis and reduction of lattice sensitivity to faults

Thank you!