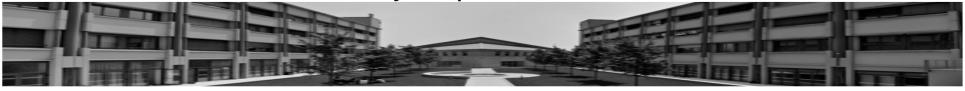


# Electronic Systems Design at the Department of Computer Science University of Verona

2<sup>nd</sup> Italian Workshop on Embedded Systems Roma, Italy September 7-8, 2017





- The emerging IT scene
- Embedded systems design
- Networked embedded systems design
- Embedded systems verification
- Projects
- Teaching at University of Verona
- Spin-off





# The Emerging IT Scene

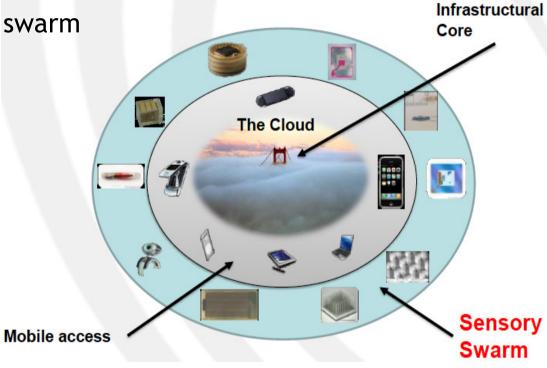
### A continuous of:

smart devices: the sensory swarm

- interconnection
- computational resources

### Open issues:

- Modeling
- Design
- Validation
- Interfaces generation



### Possible answer:

Moving design techniques from the single embedded system to the swarm





# **Embedded Systems Design**

Nicola Bombieri, Franco Fummi, Graziano Pravadelli, Davide Quaglia









Federico Busato,

Enrico Fraccaroli,

Michele Lora





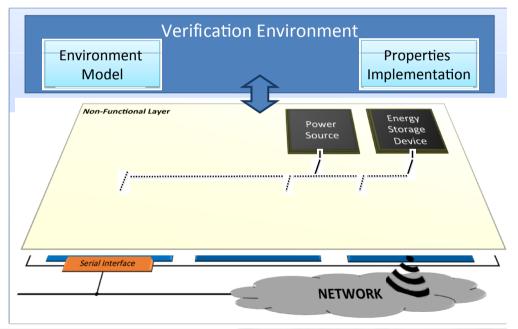






# Virtual Platform Composition

- A virtual platform is a simulation model of an actual platform. It is fundamental for:
  - concurrent hardware software co-design
  - design space exploration
  - design validation
- Investigated issues:
  - Automatic translation of heterogeneous models into an homogeneous representation
  - Fast simulation
  - Re-design
  - Interfaces generation



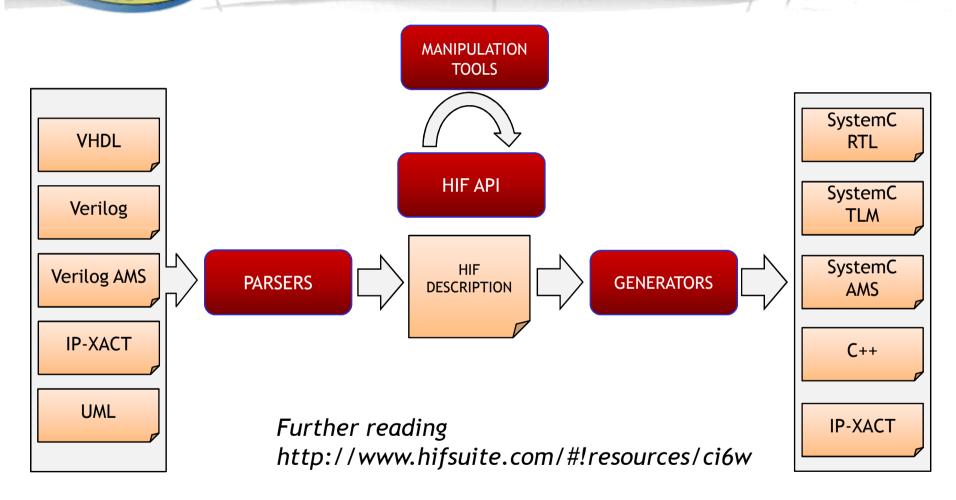


# Recent publications

- Vinco Sara, Guarnieri Valerio, Fummi Franco (2015). Code Manipulation for Virtual Platform Integration. IEEE TRANSACTIONS ON COMPUTERS, p. 1-14, ISSN: 0018-9340, doi: 10.1109/TC.2015.2500573
- E. Fraccaroli, M. Lora, S. Vinco, D. Quaglia and F. Fummi (2016). Integration of mixed-signal components into virtual platforms for holistic simulation of smart systems, DATE, Dresden, 2016, pp. 1586-1591.
- Nicola Bombieri, Franco Fummi, Sara Vinco (2015). A Methodology to Recover RTL IP Functionality for Automatic Generation of SW Applications. ACM TRANSACTIONS ON DESIGN AUTOMATION OF ELECTRONIC SYSTEMS, vol. 20, p. 1-25, ISSN: 1084-4309, doi: 10.1145/2720019
- Luigi Di Guglielmo, Franco Fummi, Graziano Pravadelli, Francesco Stefanni, Sara Vinco (2013). UNIVERCM: The UNIversal VERsatile Computational Model for Heterogeneous System Integration. IEEE TRANSACTIONS ON COMPUTERS, vol. 62, p. 225-241, ISSN: 0018-9340, doi: 10.1109/TC.2012.156
- A. Acquaviva, N. Bombieri, F. Fummi, S. Vinco (2013). Semi-Automatic Generation of Device Drivers for Rapid Embedded Platform Development. IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, vol. 32, p. 1293-1306, ISSN: 0278-0070, doi: 10.1109/TCAD.2013.2257924
- N. Bombieri, F. Fummi, G. Pravadelli (2011). Automatic Abstraction of RTL IPs into Equivalent TLM Descriptions. IEEE TRANSACTIONS ON COMPUTERS, vol. 60, p. 1730-1743, ISSN: 0018-9340, doi: 10.1109/TC.2010.187











# Parallel Embedded Software

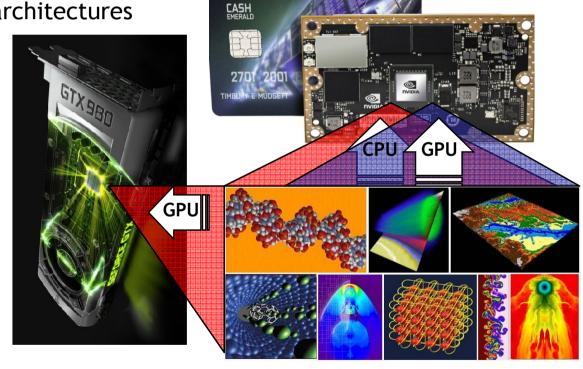
Synergism of parallelism in the algorithm, application program and computer architecture development.

• Parallelism and parallel architectures

- CUDA, OpenCL, OpenACC
- OpenMP, MPI
- Performance analysis
- Optimization

### Investigated issues:

- GPU programming
- Heterogeneous CPU-GPU architectures
- Power-aware performance tuning







# Recent publications

- F. Busato, N. Bombieri, BFS-4K: an Efficient Implementation of BFS for Kepler GPU Architectures. In «IEEE Transactions on Parallel and Distributed Systems» vol.26, n.7, pp. 1826-1838, 2015
- N. Bombieri, F. Busato, F. Fummi, Pro++: A Profiling Framework for Primitive-based GPU Programming. Preprint on IEEE Transactions on Emerging Topics in Computing, 2016
- N. Bombieri, R. Distefano, G. Scardoni, F. Fummi, C. Laudanna, R. Giugno, Dynamic modeling and simulation of leukocyte integrin activation through an electronic design automation framework. In Proceedings of "Conference on Computational Methods in Systems Biology (CMSB)", Manchester, UK, 17-19 November, 2014, pp. 1-12





### Graph analysis through GPU architectures:

- BFS-4K (parallel BFS graph visiting)
- H-BF (parallel single-source-shortest paths)

### Biological network analysis on multicore/manycores:

- APPAGATO: Approximate parallel and stochastic graph queying tool for GPU architectures
- GRAPES: a Software for Parallel Searching on Biological Graphs targeting Multi-core Architectures
- BIODEA/SyQUAL: an EDA framework for modeling and simulation of biological networks

### Primitive-based GPU programming:

- Pro++: A Profiling Framework for Primitive-based GPU Programming
- MIPP: A Microbenchmark Suite for Performance, Power, and Energy Consumption Characterization of GPU architectures



- HW security: trojan detection, vulnerability analysis
- Internet of Things for healthcare and ambient assisted living

Graziano Pravadelli Florenc Demrozi









## Networked embedded systems design

Enrico Fraccaroli, Franco Fummi, Davide Quaglia, Gabriele Miorandi













# Networked Embedded Systems

Networked embedded systems (NES) are small, intelligent, embedded systems able to communicate each other and with Internet

### Key terms

- Internet of Things
- Machine-to-machine
- Smart systems

#### Miniature 9-Axis Inertial Module with 32-bit Processing Unit

MEMS leader unveils a compact 9 degrees-of-freedom motionsensing module with powerful processing capabilities

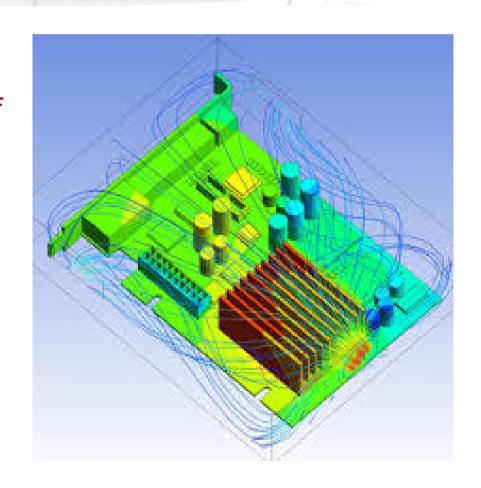






# Modeling & Simulation of NES

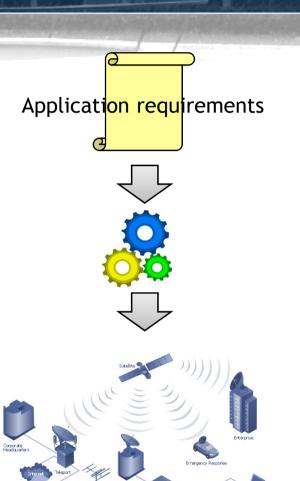
- This research topic regards the creation of models and simulation of
  - Digital hardware
  - Network (e.g., WiFi)
  - Analogue hardware
  - MEMS
  - Physical components belonging to several domains: mechanical, thermal, optical, etc.
- Languages
  - UML
  - SystemC



# COIS. KIS

# Network synthesis

- Automatic methodology to design the network infrastructure
  - Topology
  - Nodes (number, type)
  - Channel types
  - Protocols
- Optimal allocation of resources with respect to given metrics (e.g., cost, bandwidth, delay, robustness)
- Needed to address the challenging size and heterogeneity of future's networks

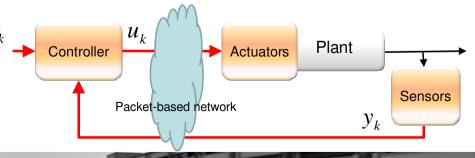




# Design and Verification of Networked Control Systems

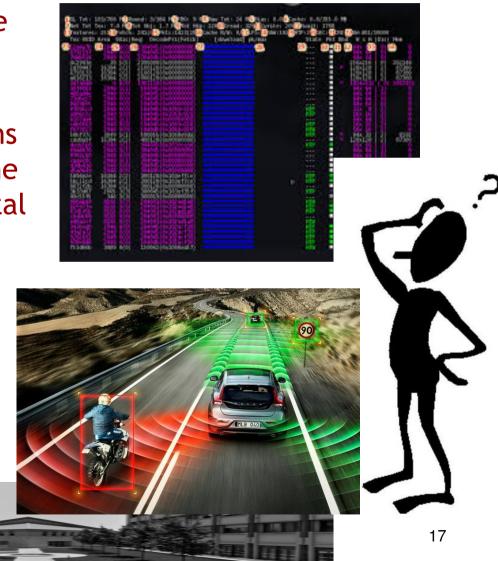
- Physical systems controlled through a packet-based network
- Applications
  - Tele-operation
  - Automotive
- Joint design of the controller and of the network
- Network protocols are implemented as software in applications and operating system
- Automatic verification of protocol implementation through observation of
  - Simulation traces
  - Actual behavior





# **Functional Safety of NES**

- Many network aspects are now intertwined with embedded systems
- Extension of investigations on functional safety to the interaction between digital HW, SW and network
- Automatic verification of network-related SW implementation through observation of
  - Simulation traces
  - Actual behavior





# Recent publications

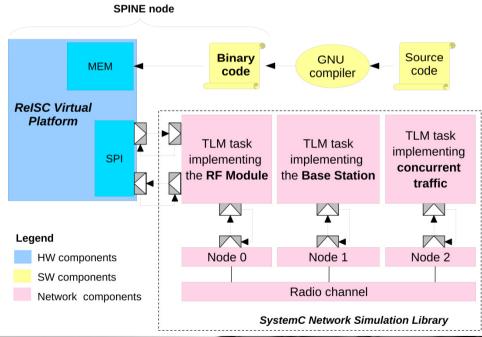
- R. Muradore, D. Quaglia, Communication-Aware Bandwidth-Optimized Predictive Control of Motor Drives in Electric Vehicles, IEEE Transactions on Industrial Electronics, vol. 63, n. 9, September 2016, pp. 5602-5611.
- Riccardo Muradore, Davide Quaglia, Energy-Efficient Intrusion Detection and Mitigation for Networked Control Systems Security, IEEE Transactions on Industrial Informatics, vol. 11, n. 3, June 2015, pp. 830-840, DOI 10.1109/TII.2015.2425142.
- Emad Ebeid, Franco Fummi, and Davide Quaglia, Model-Driven Design of Network Aspects of Distributed Embedded Systems, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 34, n. 4, April 2015, pp. 603-614.
- Parinaz Sayyah, Mihai T. Lazarescu, Sara Bocchio, Emad Ebeid, Gianluca Palermo, Davide Quaglia, Alberto Rosti, Luciano Lavagno, Virtual Platform-based Design Space Exploration of Power-Efficient Distributed Embedded Applications, ACM Transactions on Embedded Computing Systems, vol. 14, n. 3, April 2015, pp. 49:1-49:25, DOI 10.1145/2723161.
- R. Muradore, L. Repele, D. Quaglia, P. Fiorini, Improving Performance of Networked Control Systems by using Adaptive Buffering, IEEE Transactions on Industrial Electronics, vol. 61, n. 9, September 2014, pp. 4847-4856.



### Tools: SCNSL

### SystemC Network Simulation Library (SCNSL)

- Extension of SystemC to simulate packet-based networks
- Provides modeling primitives for:
  - Packet transmission/reception
  - Channel contention
  - Wireless path loss
  - Antenna modeling
- Simplify the connection to a virtual platform





# **Embedded Systems Verification**

Franco Fummi, Graziano Pravadelli, Tiziano Villa







Alessandro Danese, Luca Geretti









(Functional) verification is the process of determining that the intent of the designer has been correctly implemented and is preserved during the implementation process

Design

Design

specification

Design

intent

 Does my specification really match my intent?

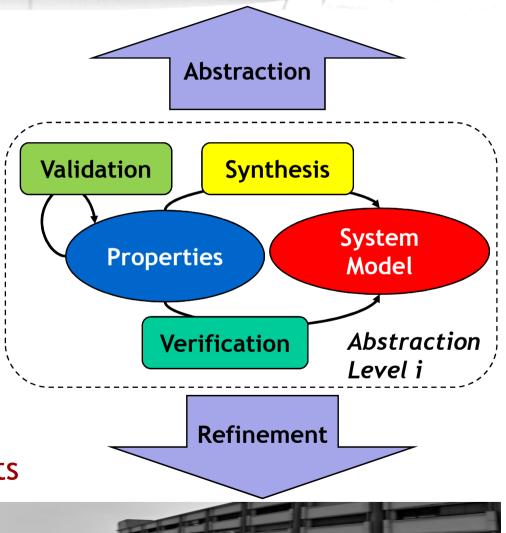
 Does my implementation really match my specs?

Assertion Based Verification (ABV) provides a unified methodology for <u>unambiguously specifying and verifying</u> design intents by using formal specifications





- Design is a continuous mix of verification, refinement and abstraction
- Verification should not be only a post-refinement step, but it should guide the design with some correct-by-construction refinements





### Verification: how?

- Mainly based on the definition and verification of assertions
- We consider two classes of assertions: spatial and temporal
  - Spatial assertions are the most generic ones, and apply to cyber-physical systems which are modeled to fully capture the interaction between the analog (environment) and the digital (controller) world
  - Temporal assertions are a very relevant subclass, where we decide to focus on timed dynamics; such simplification allows us to identify more complex relationships



# Spatial assertions: challenges

- Deal with approximation error in a formally sound way
- Control of approximation error, especially when non-determinism is considered
- Efficient representation of space regions, due to a significant impact of dimensionality
- Effective convergence for infinite-time reachability calculus
- Combine different approaches to different classes of dynamics

# To I se i to i

# Temporal assertions: challenges

- Automatic generation of assertions
- Automatic abstraction and refinement (reuse) of assertions at different levels (ESL, TLM, RTL)
- Evaluation of the quality of assertions
- Verification of assertions taking care of:
  - dynamic vs. static approaches
  - discrete vs. continuous domains
  - real time constraints
- Non only in the functional domain (power, timing, ...)



# Recent publications

- Tiziano Villa, Alexandre Petrenko, Nina Yevtushenko, Alan Mishchenko, Robert K. Brayton: Component-Based Design by Solving Language Equations. Proceedings of the IEEE 103(11): 2152-2167 (2015)
- Pierluigi Nuzzo, Alberto L. Sangiovanni-Vincentelli, Davide Bresolin, Luca Geretti, Tiziano Villa: A Platform-Based Design Methodology With Contracts and Related Tools for the Design of Cyber-Physical Systems. Proceedings of the IEEE 103(11): 2104-2132 (2015)
- Luca Benvenuti, Davide Bresolin, Pieter Collins, Alberto Ferrari, Luca Geretti, Tiziano Villa: Assume-guarantee verification of nonlinear hybrid systems with Ariadne, Int. J. Robust Nonlinear Control 2014; 24:699-724
- Alessandro Danese, Graziano Pravadelli, Ivan Zandona: Automatic generation of power state machines through dynamic mining of temporal assertions. DATE 2016
- Alessandro Danese, Tara Ghasempouri, Graziano Pravadelli: Automatic extraction of assertions from execution traces of behavioural models. DATE 2015
- Nicola Bombieri, Riccardo Filippozzi, Graziano Pravadelli, Francesco Stefanni: RTL property abstraction for TLM assertion-based verification. DATE 2015
- F. Fummi, G. Pravadelli, D. Quaglia, S. Vinco, Semiformal Assertion-Based Verification of Hardware/Software Systems in a Model-Driven Design Framework, chapter in "Handbook of Hardware/Software Codesign", edited by Soonhoi Ha and Jürgen Teich, Springer, to be published in 2017.

# Tools

- Ariadne: Formal analysis of hybrid systems modeled by hybrid automata
- BALM-II: Component-based synthesis of sequential systems
- ODEN / A-TEAM: tools for automatic generation of temporal assertions from simulation traces. A-TEAM is the evolution of ODEN with customizable templates for the extraction of assertions.
- TURBO / MANGROVE: GPU-enabled tools for the automatic extraction of invariants
- IBATPG (invariant-based ATPG): test sequences generator based on invariant mining
- SPLINTER: injector of faults (stuck-at and mutants) and trojans





# **Projects**





# Large Related EU Projects

- ANGEL
  - mobile gateway for sensors network
- VERTIGO
  - HW formal verification
- - embedded systems design and verification
- - control for coordination of distributed systems
- TOUCHMORE
  - correct software generation for multicore platform
- **SOURCE** COMPLEX
  - codesign and power management in PLatform-based design
- SMAC
  - smart components and Smart Systems integration
- CONTREX
  - design of embedded mixed-criticality control systems











# **Teaching activity at University of Verona**





### Master Degree in Computer Science and Engineering

- Curriculum in Embedded Systems
- about 20 students this year





# Spin-off



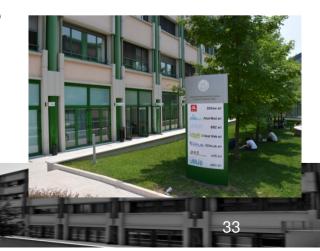




- ▶ Founded in 2007
- Located at the Computer Science Park of University of Verona
- 15 active persons:
  - 6 Co-founders (3 from ESD)
  - 6 Employees
  - 3 Collaborators
- Engineering and commercialization of the ESD research products
- Employment opportunity for graduated students and PhD



www.edalab.it





# **Events in Verona in September**





- Summer School on Formal Methods for Cyber-Physical Systems
  - Edition 2017: Automatic Synthesis of Controllers for Hybrid Systems
  - From 12/09/2017 to 16/09/2017
  - Dipartimento di Informatica, Strada le Grazie 15, Verona (Italy)
  - <a href="https://cps-2017.di.univr.it/school-editions/2017">https://cps-2017.di.univr.it/school-editions/2017</a>
- FDL 2017 Forum on specification & Design Languages
  - September 18-20, 2017
  - Accademia di Agricoltura Scienze e Lettere, Verona (Italy)
  - https://ecsi.org/fdl











