Karlsruher Institut für Technologie

Preemptable Partial Reconfiguration for Real-Time Computing with FPGAs

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Introduction

Computer platforms are evolving towards heterogeneous architectures:

- FPGAs
- SoCs (FPGA + Hardware processor)

These new architectures and their features are attractive for real-time systems. The most attractive feature is:

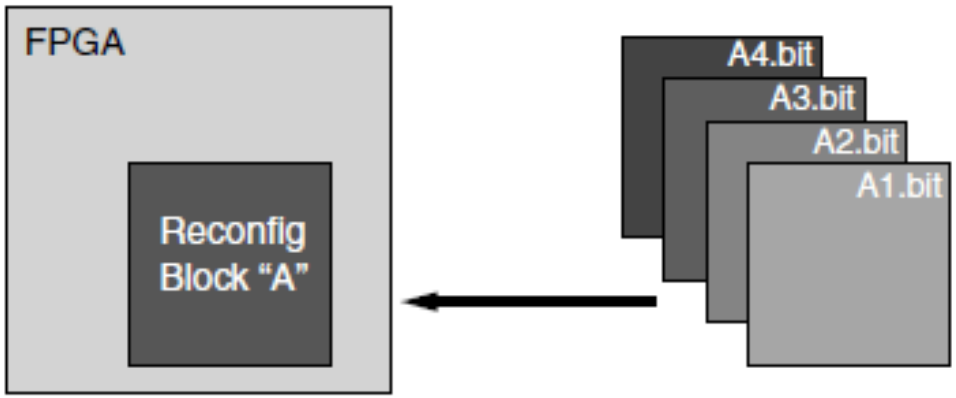
- Dynamic Partial Reconfiguration (DPR)

Introduction

Dynamic partial reconfiguration enables the possibility to reconfigure a portion of the FPGA at runtime, while the rest of the FPGA continues to operate.

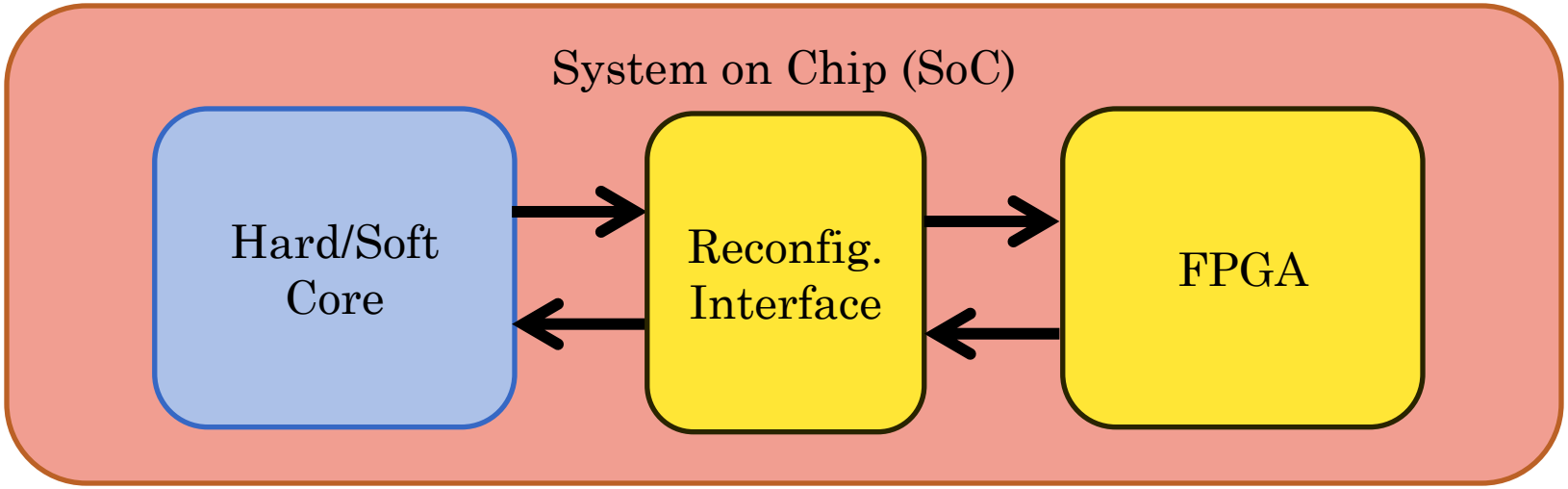
Different kind of systems can benefit from this feature to enhance the overall performance:

- Real-Time Systems
- Mixed-Criticality Systems



Introduction

The FPGA can be seen as a co-processor that exploits the hardware resources to carry out on-demand, computationally intensive tasks.



DPR allows the Core to load inside the FPGA the required hardware module only when it is necessary.

DPR Problems

Currently, the main problem is the Reconfiguration Interface.

- Each reconfiguration process must be finished or aborted.
- No possibility to resume a reconfiguration process.
- There are more than one Reconfig. Interface but only one at a time can be used.

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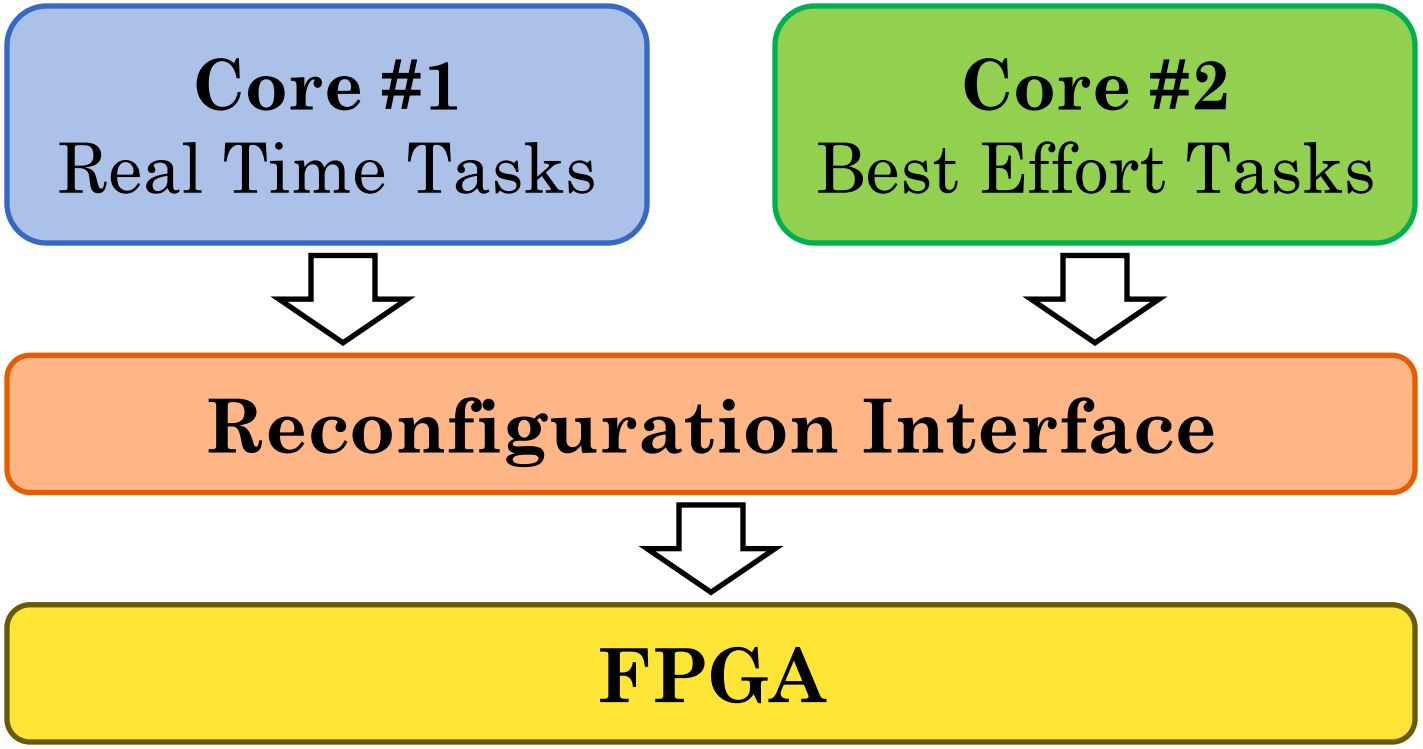
The Reconfiguration Interface is NOT PREEMPTABLE!

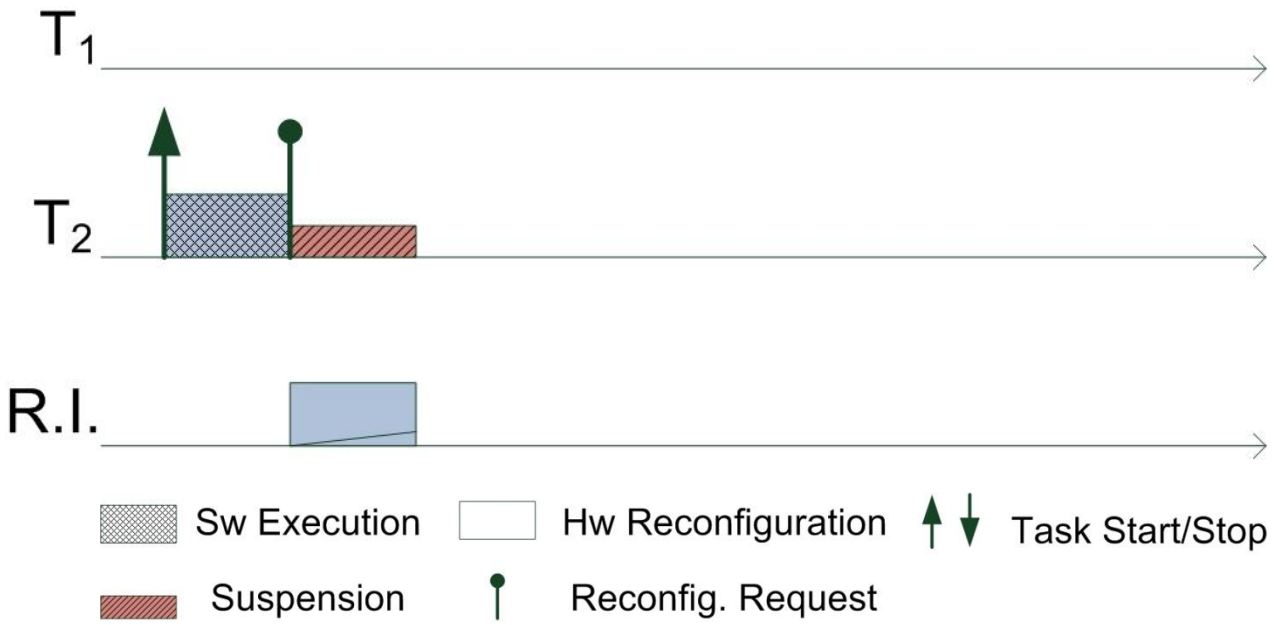
Multi Core Mixed Criticality Systems



Both RT tasks and BE tasks can trigger a hardware reconfiguration. The reconfiguration interface will be a shared resource between the two cores and among all tasks.

Priority Inversion

- SW tasks with Fixed Priority scheduling
- Each SW task can issue a hardware reconfiguration process
- Reconfiguration process can not be preempted or aborted



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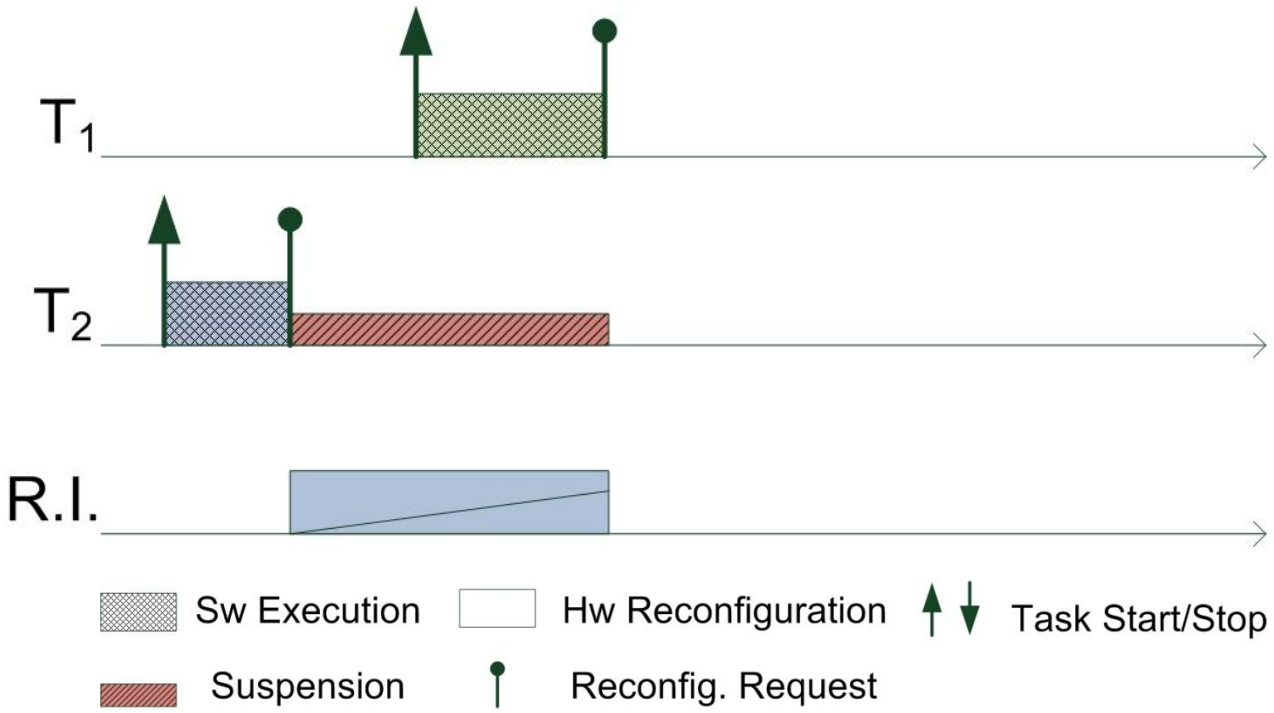

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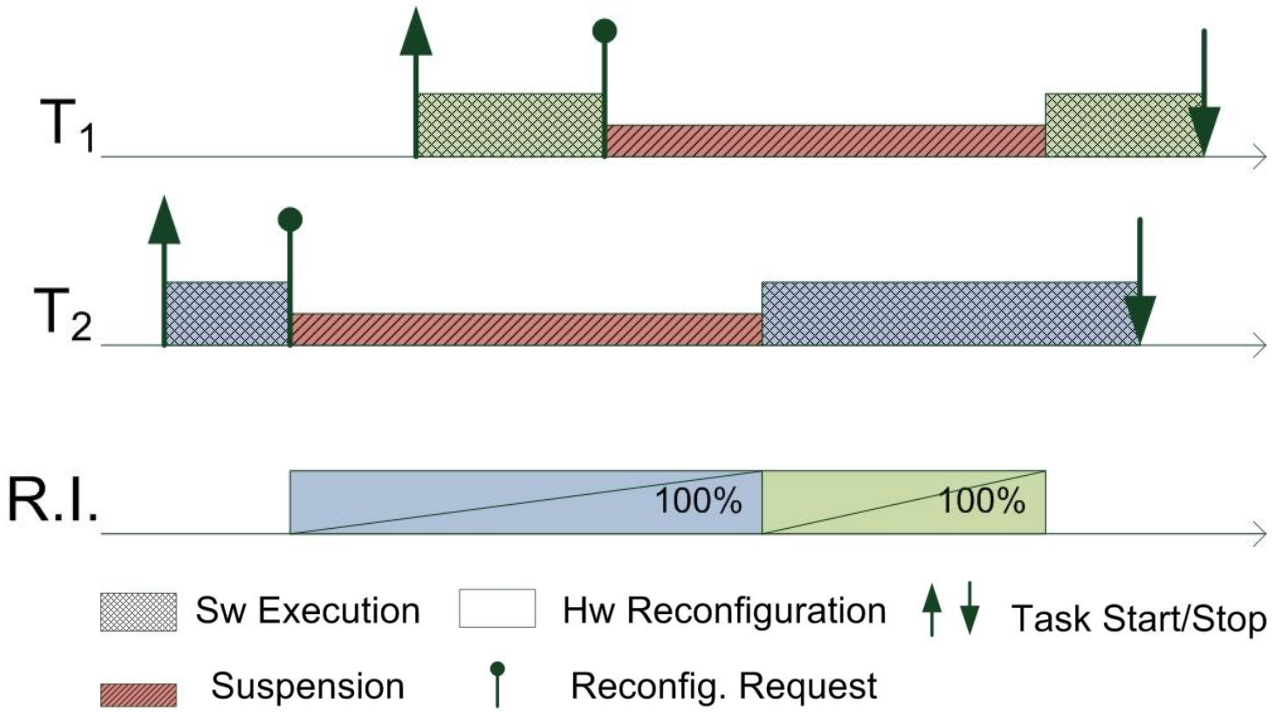

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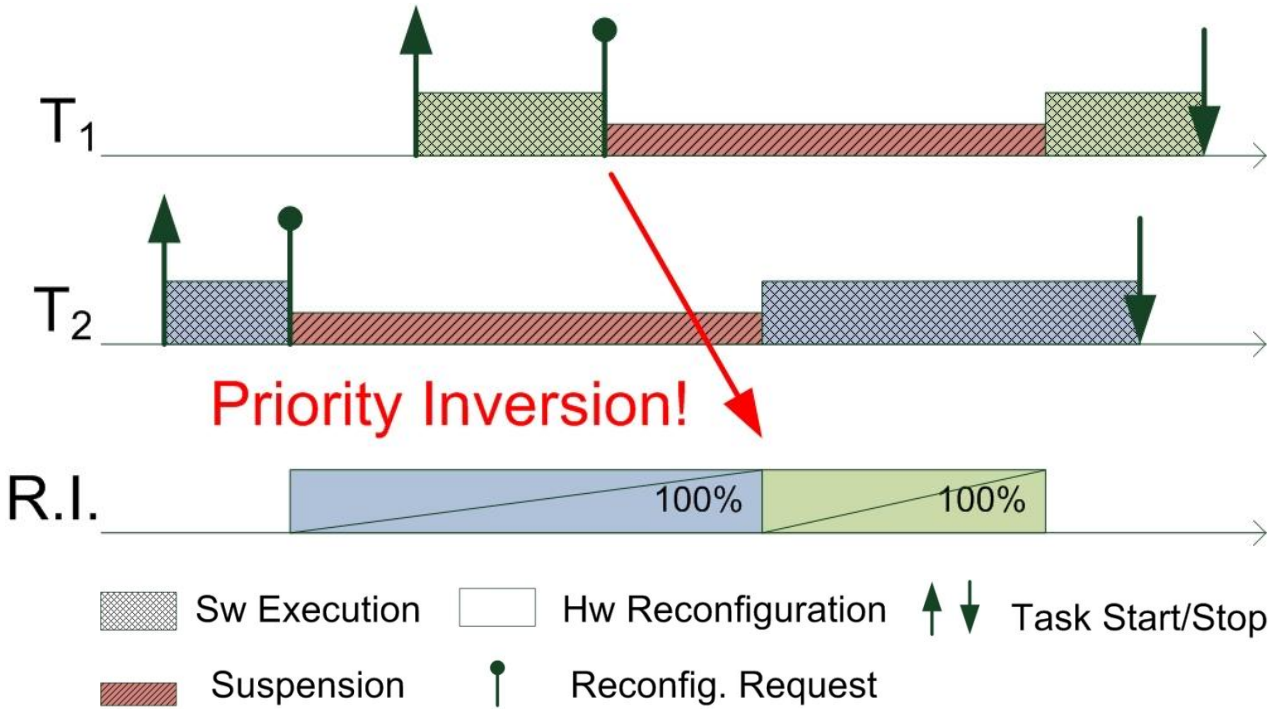

Starvation

- Real Time task (T1) has priority over Best Effort task (T2)
- The reconfiguration interface is not preemptive
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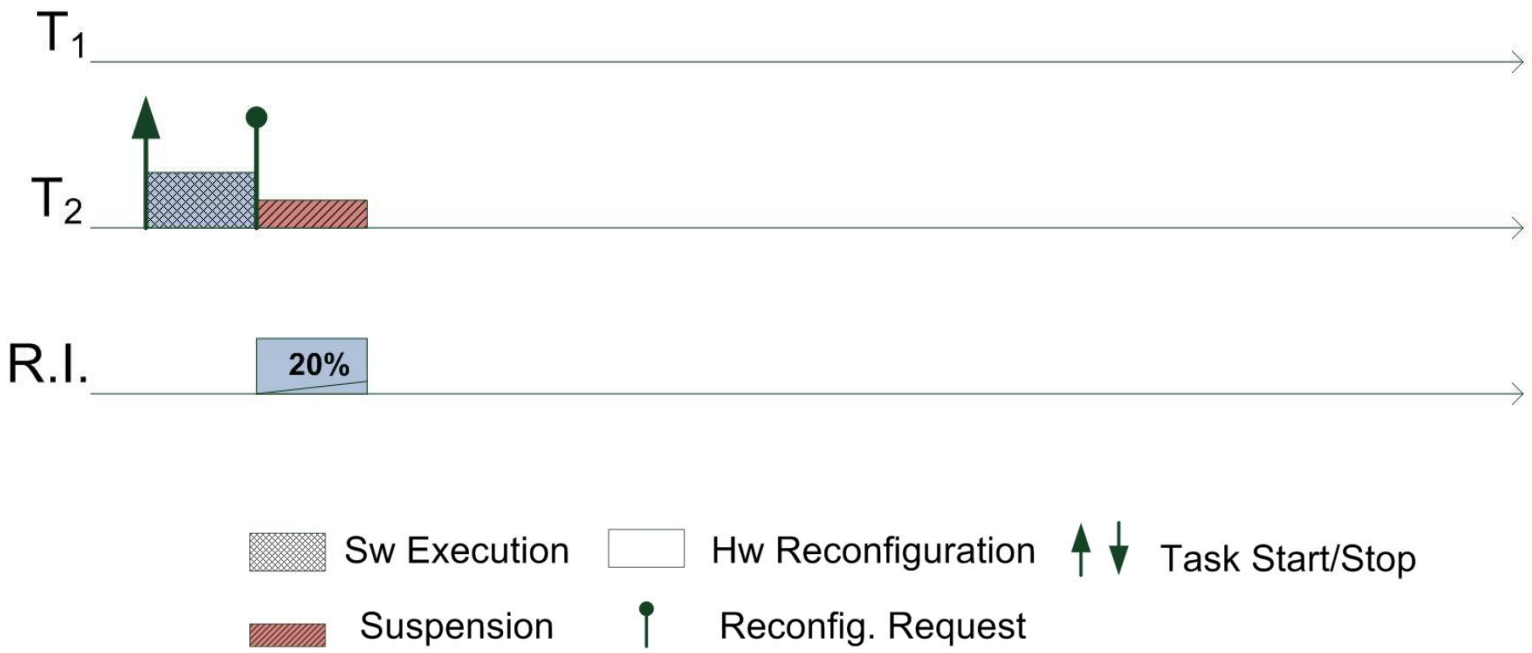
  - The reconfiguration process must be resumed from scratch



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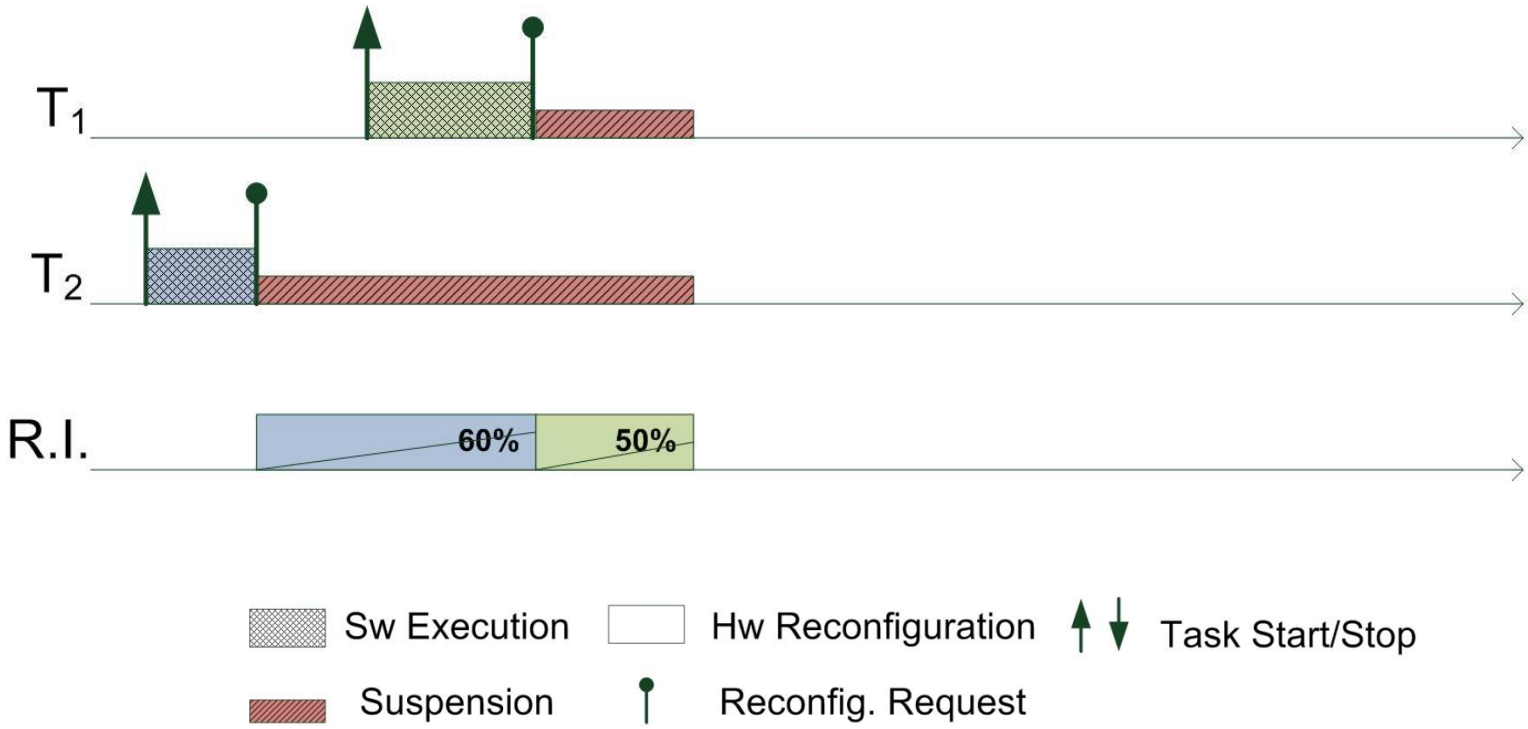

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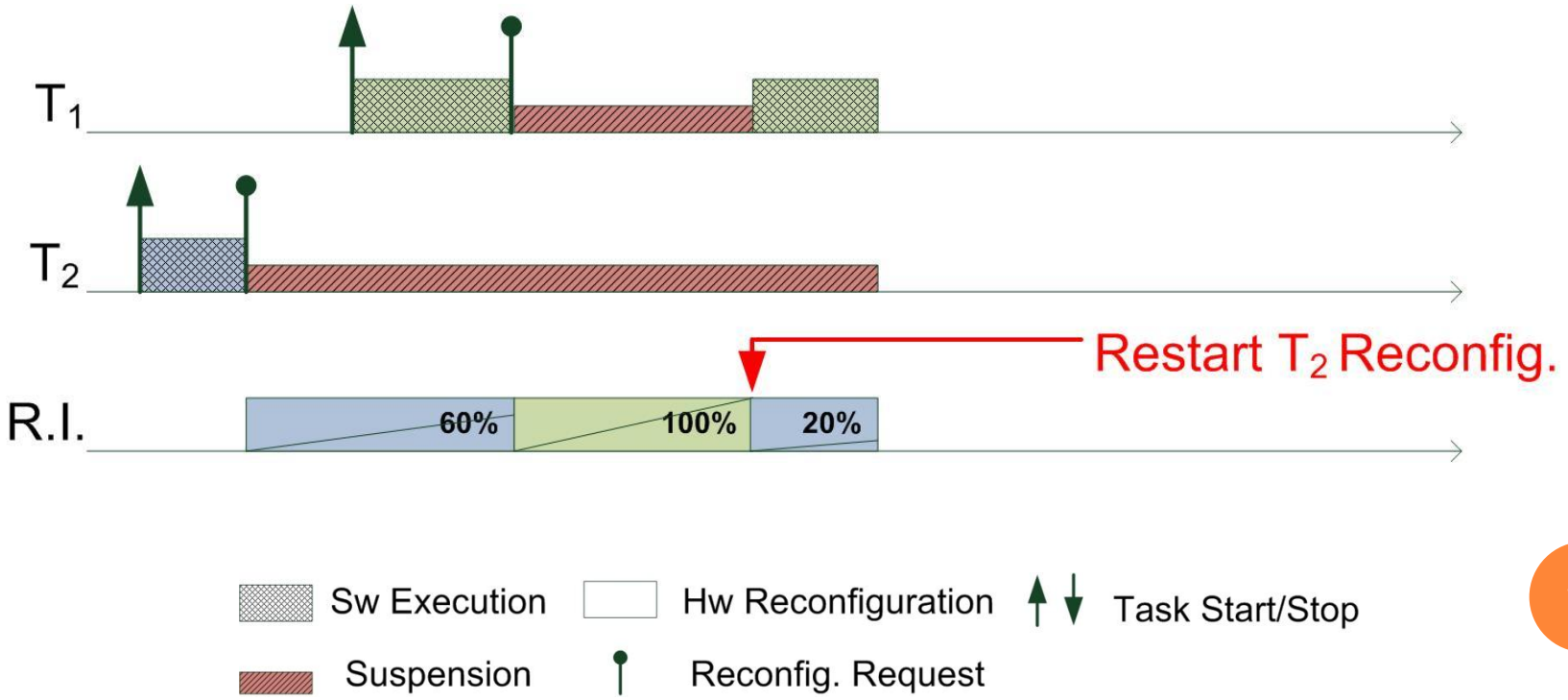

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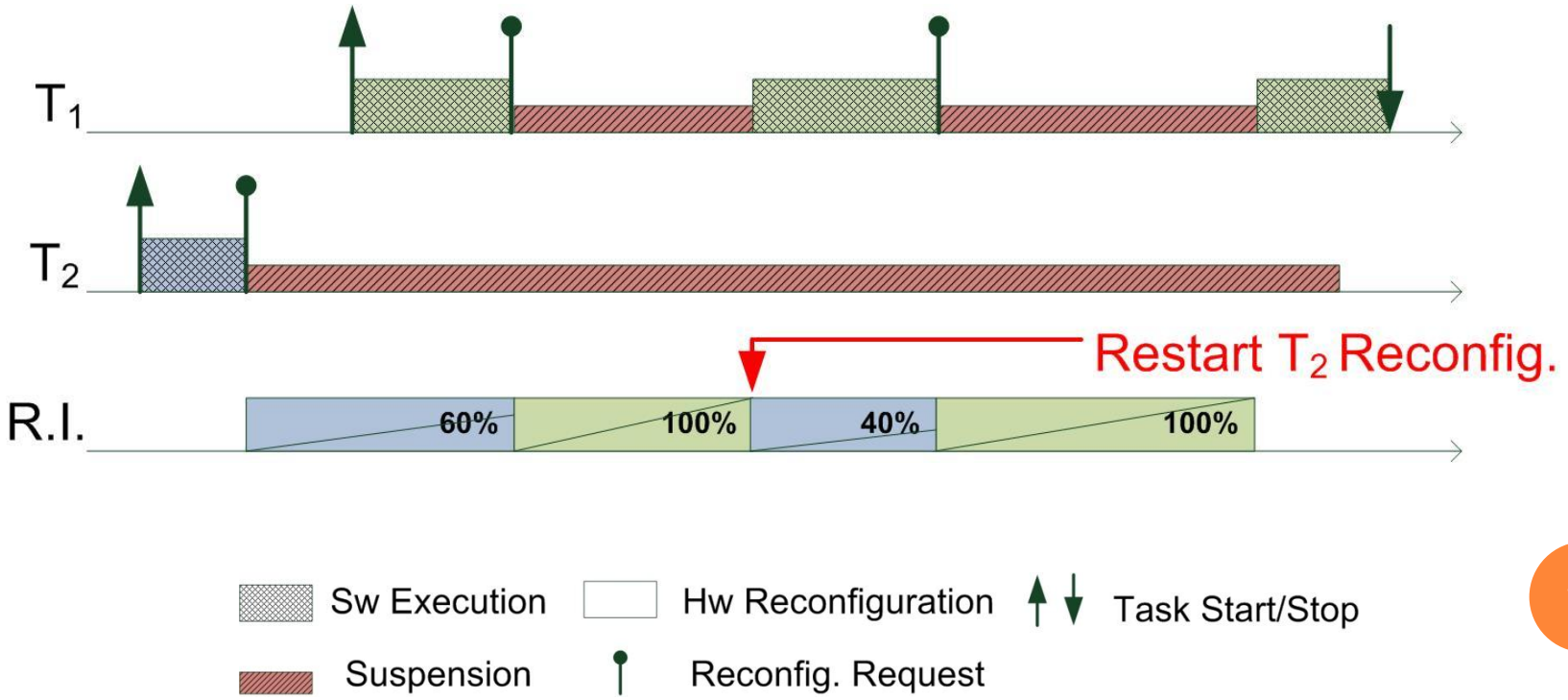

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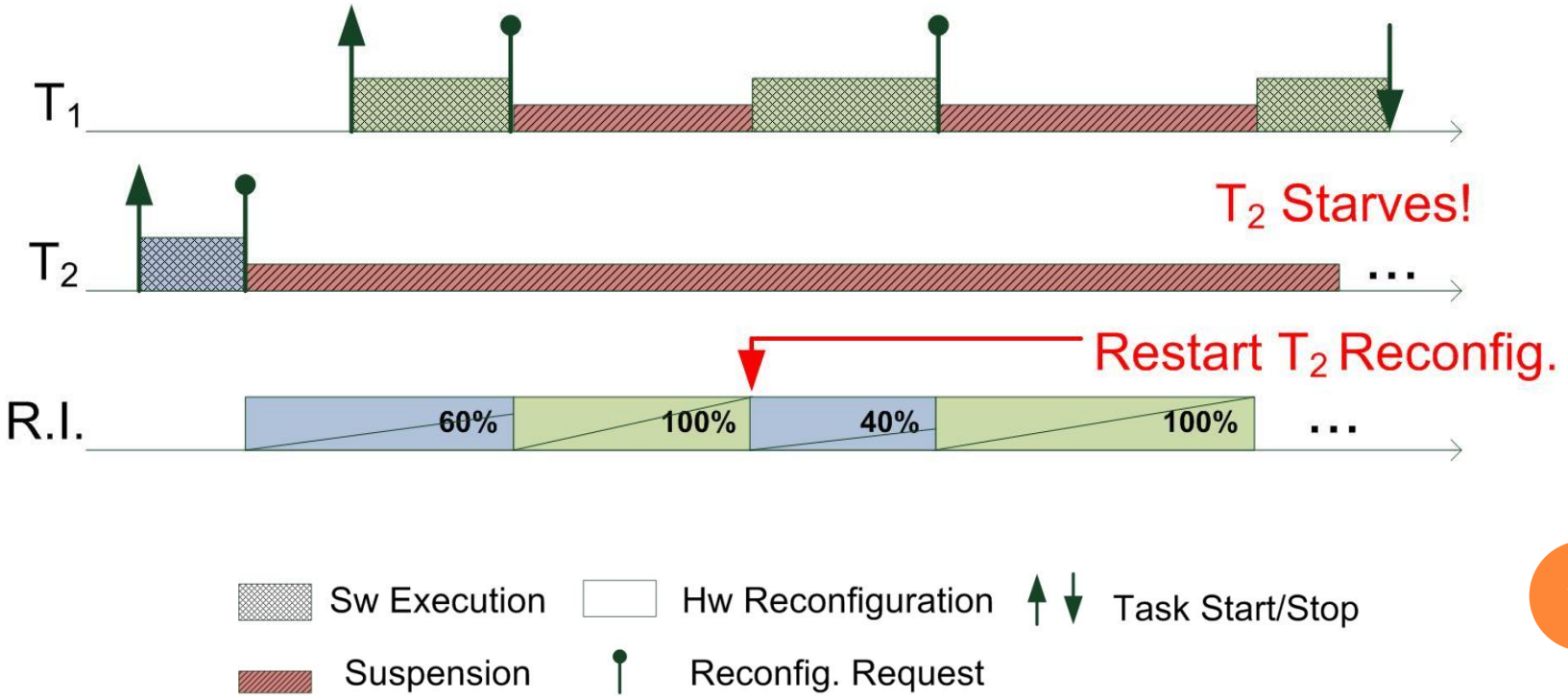


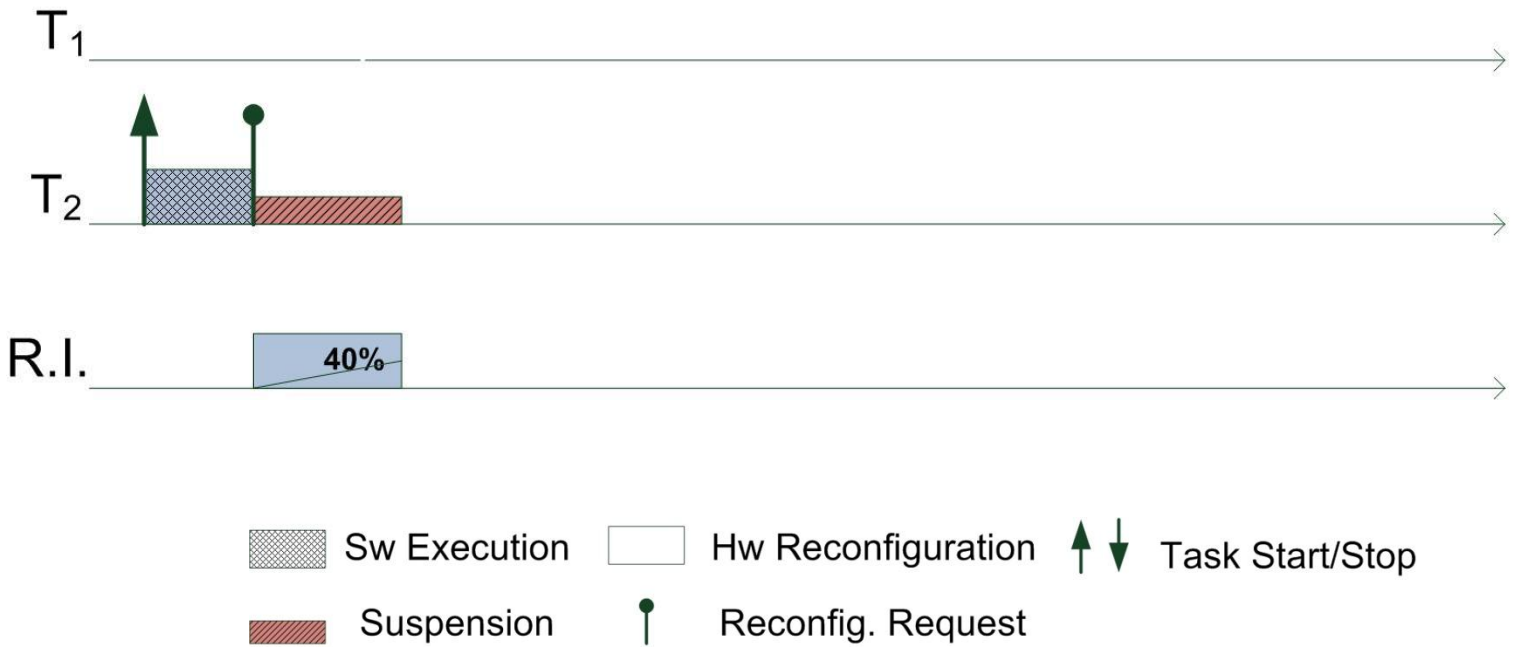
Priority Invertion and Starvation

Without a preemptable interface:

- The delay experienced by the higher priority task could be very high.
- High priority tasks could miss their deadline!
- Upper bound of the delay experienced by the Best Effort task cannot be found.

Preemptable Reconfiguration

- Real Time task (T1) has priority over Best Effort task (T2)
- The reconfiguration process is preemptable
  - Hardware reconfiguration can be resumed



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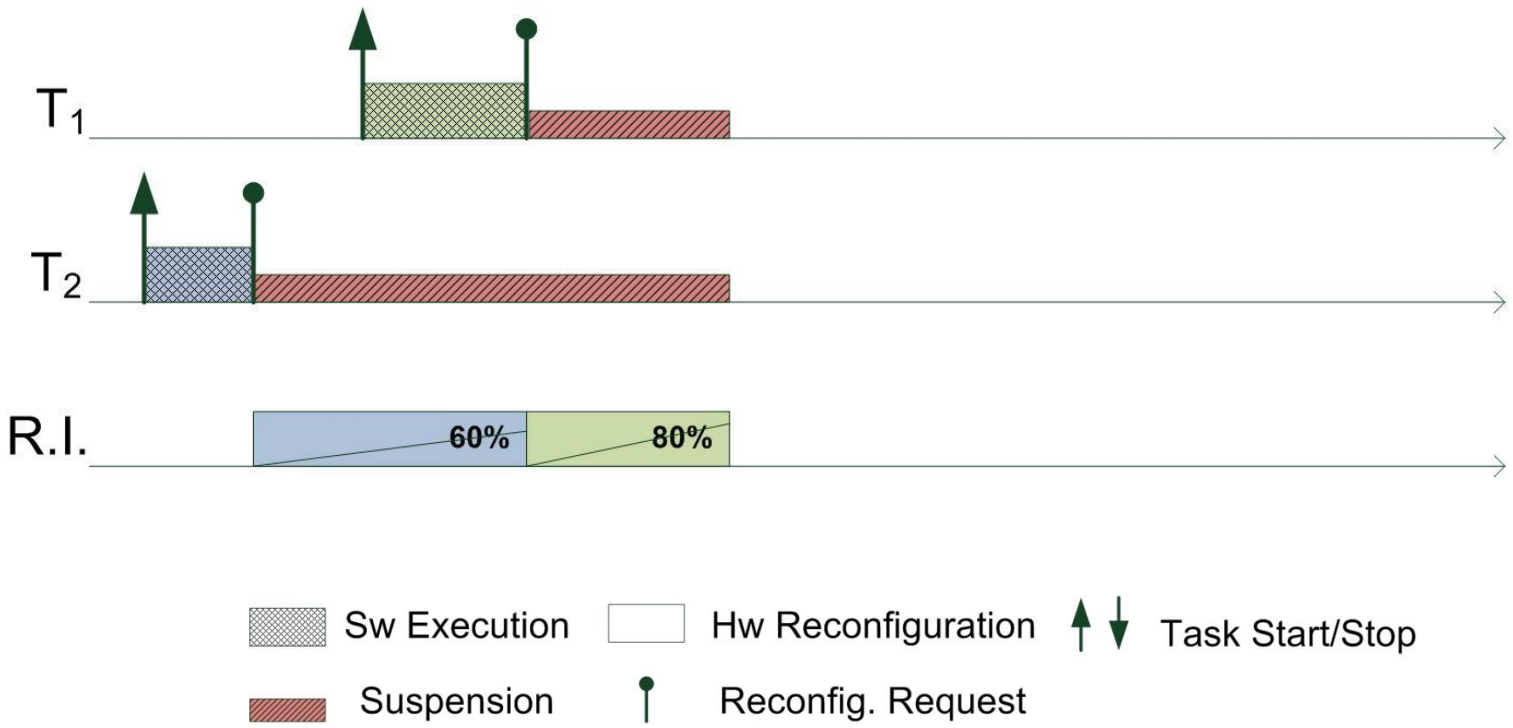

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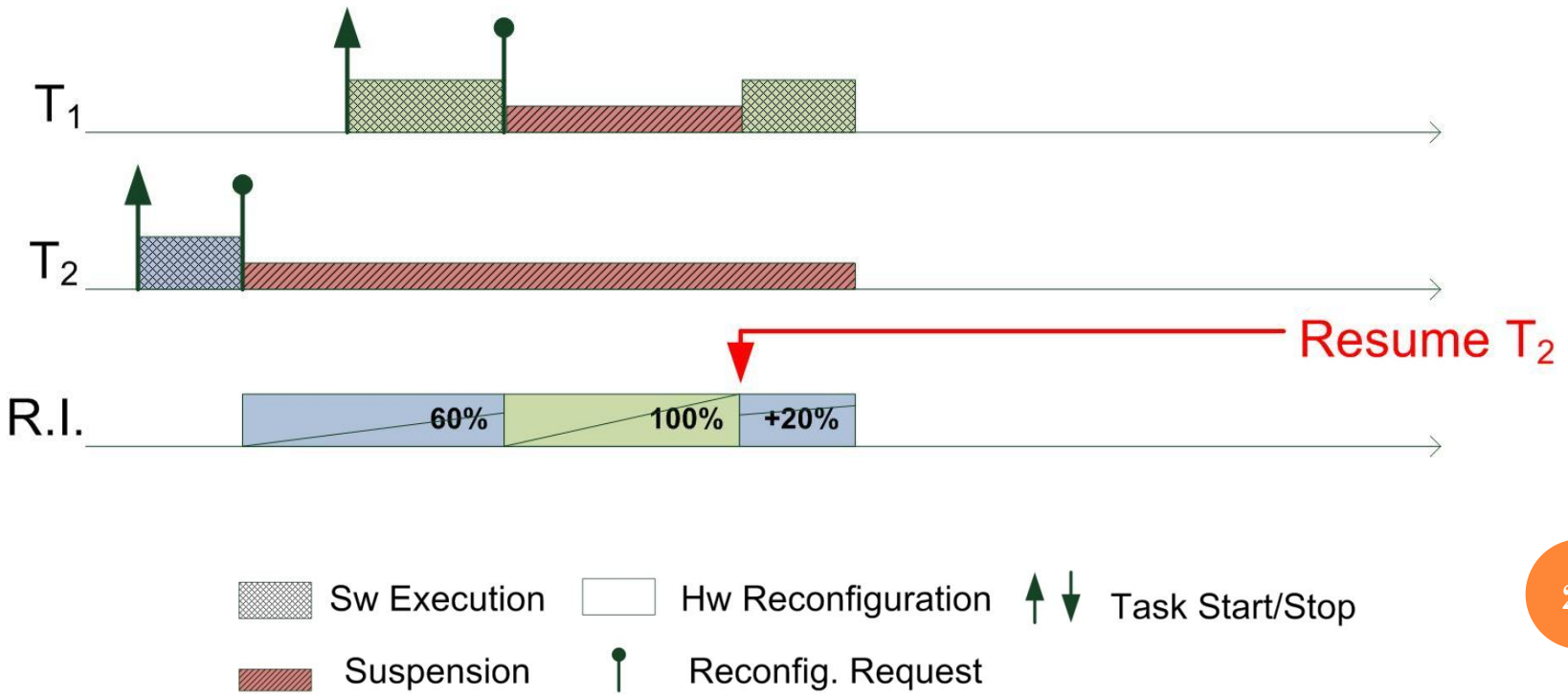

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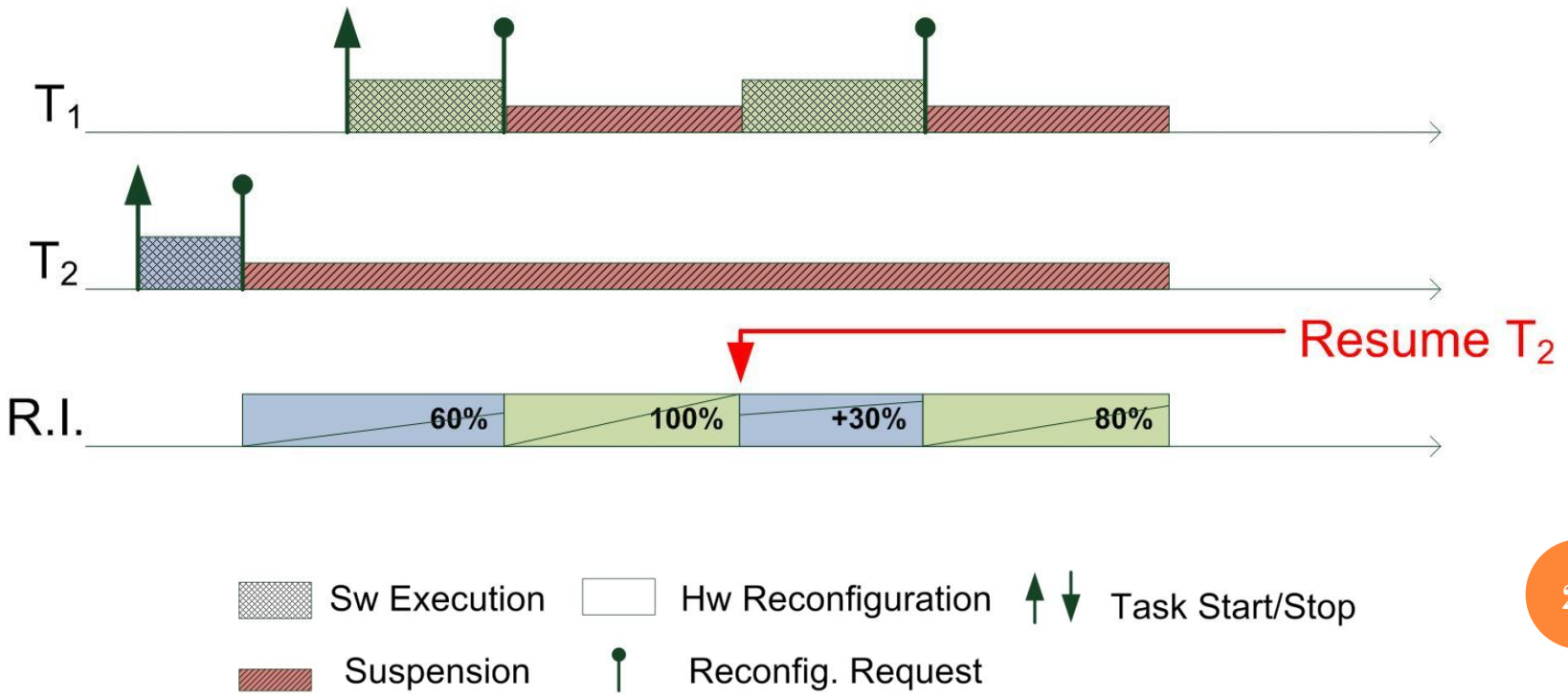

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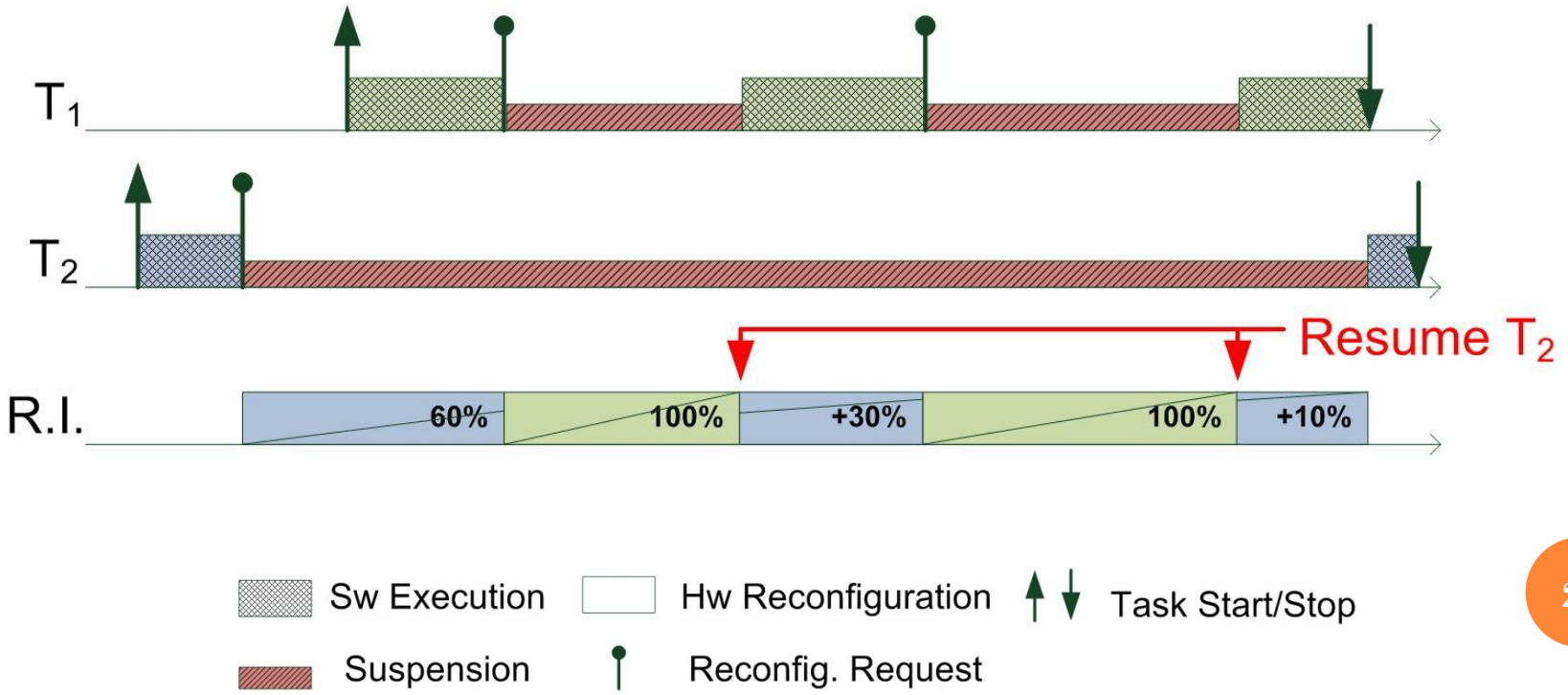


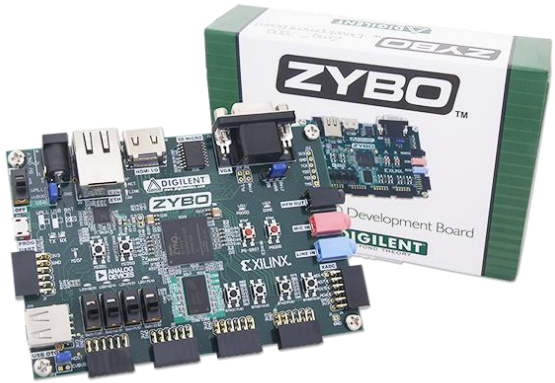
Benefits

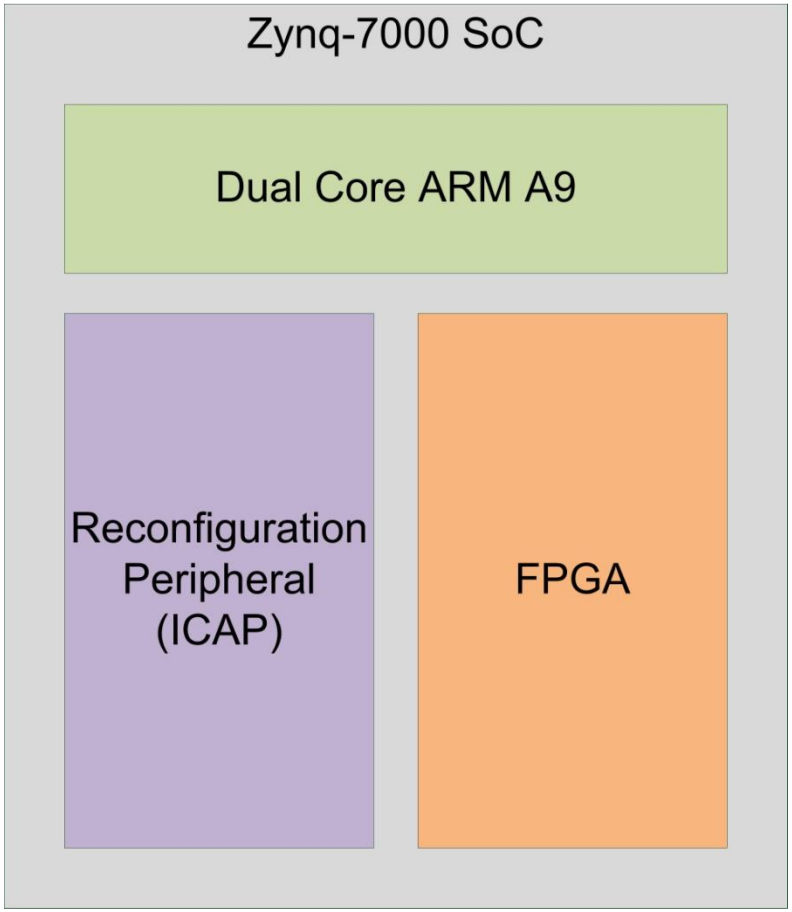
With a preemptable interface:

- Performance of both Real Time and Best Effort tasks are improved.
- The delay experienced by the higher priority task can be reduced.
- The delay experienced by Best Effort tasks can be bounded.

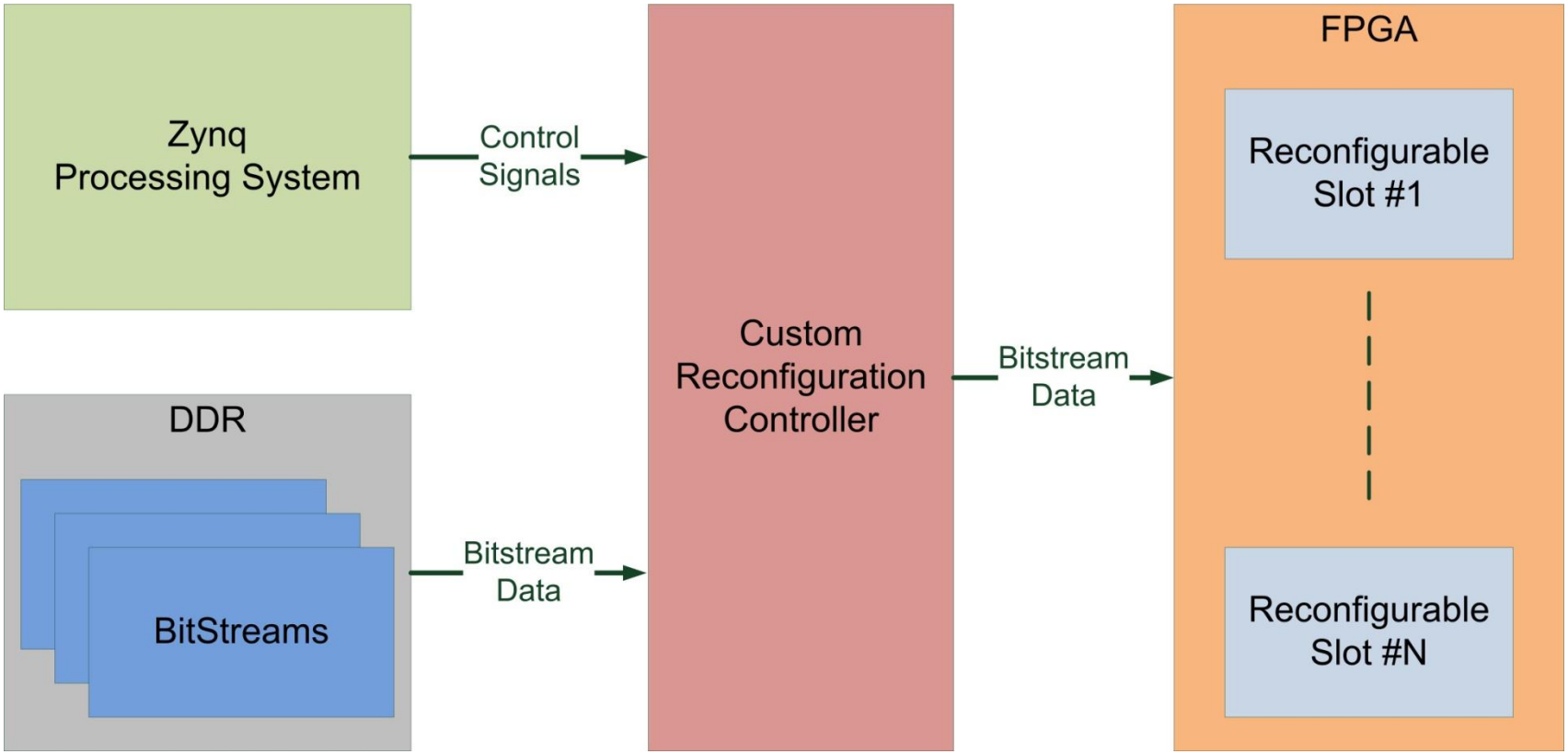
Implementation

Preemptable reconfiguration has been realized on a Xilinx Zynq-7000 platform.





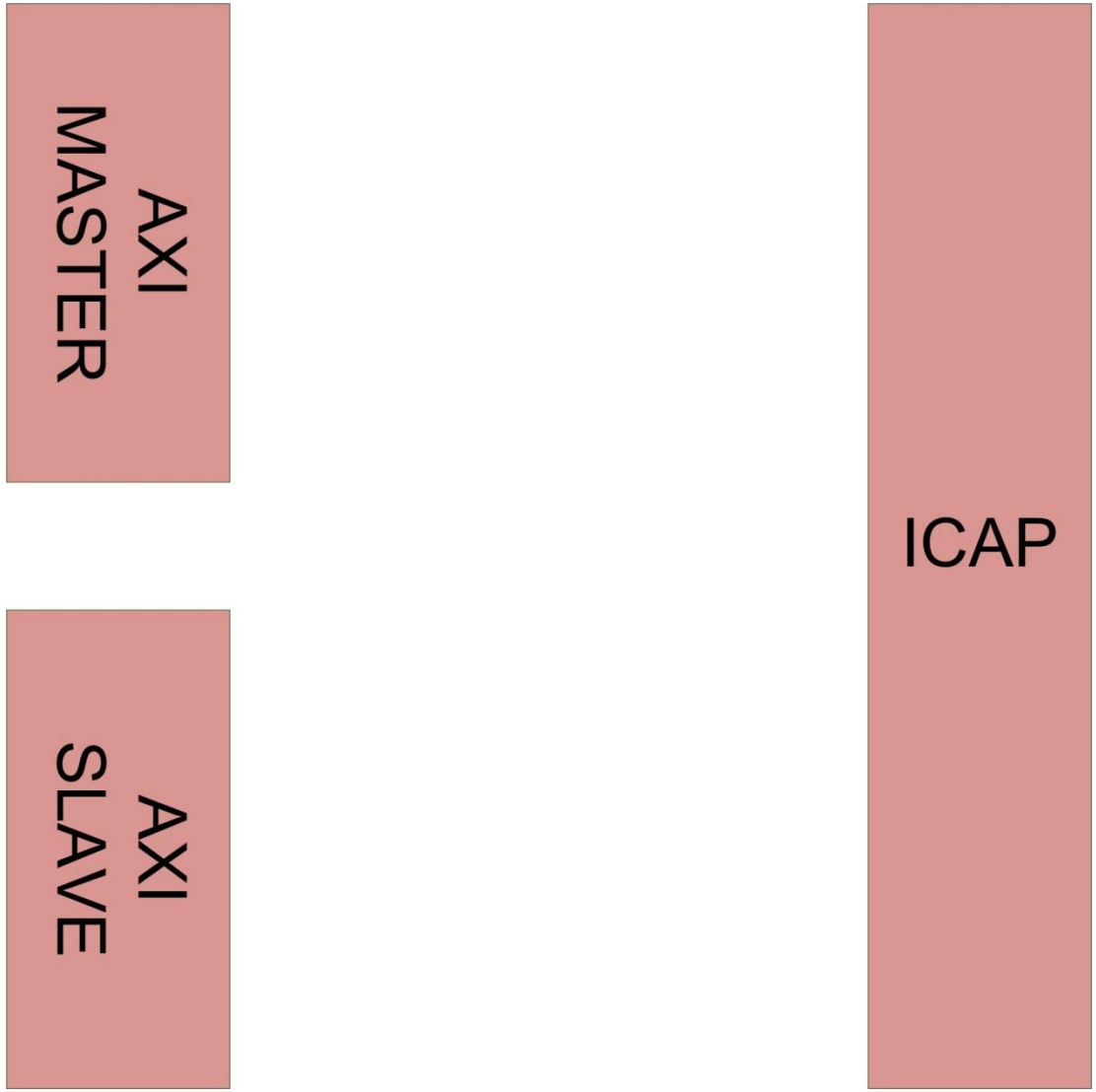
Base System Overview



- Zynq Processing System can trigger a hardware reconfiguration by sending the bitstream to configure to the Reconfiguration Controller.

Custom Reconfiguration Controller

Xilinx IP Cores



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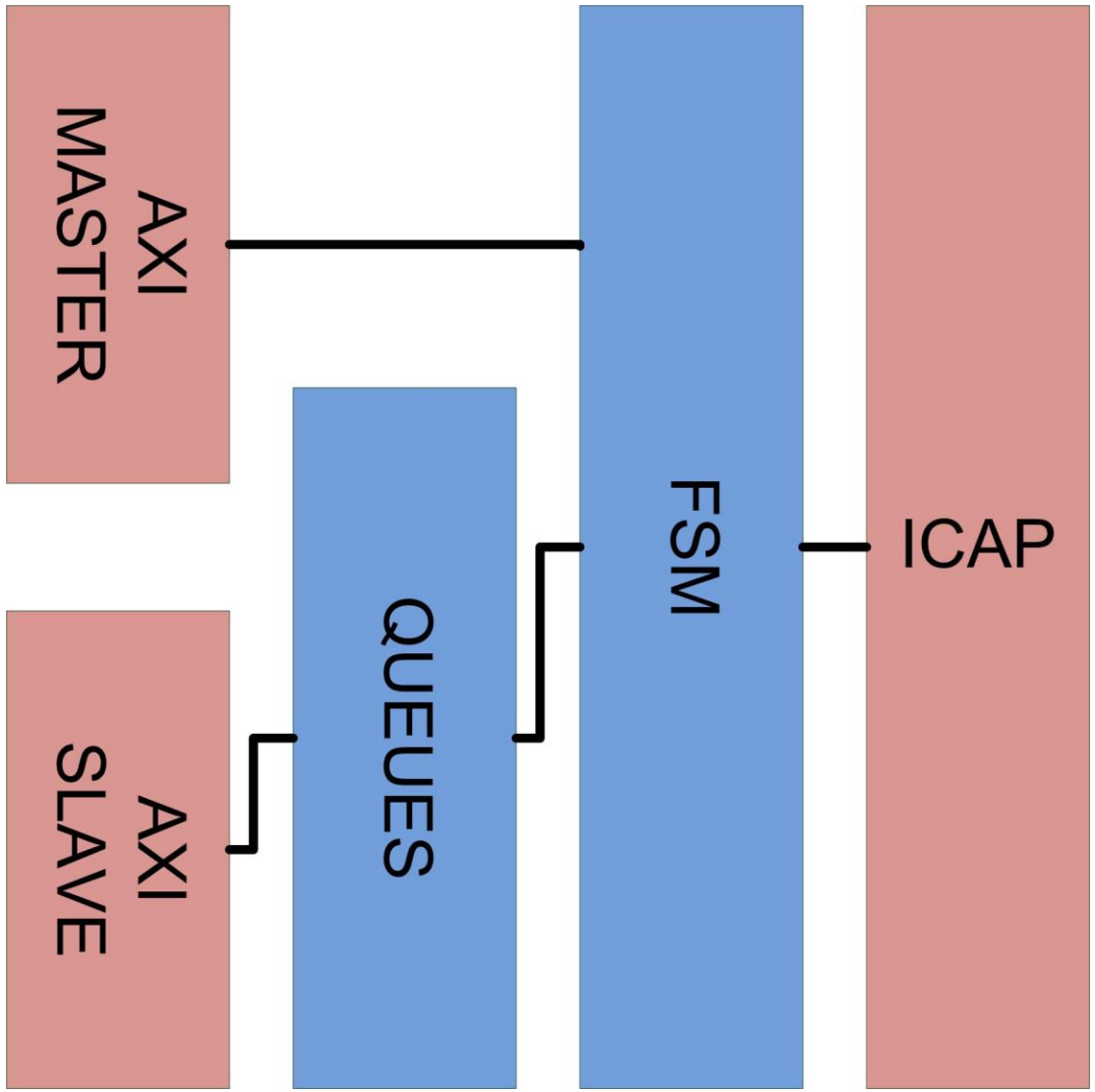
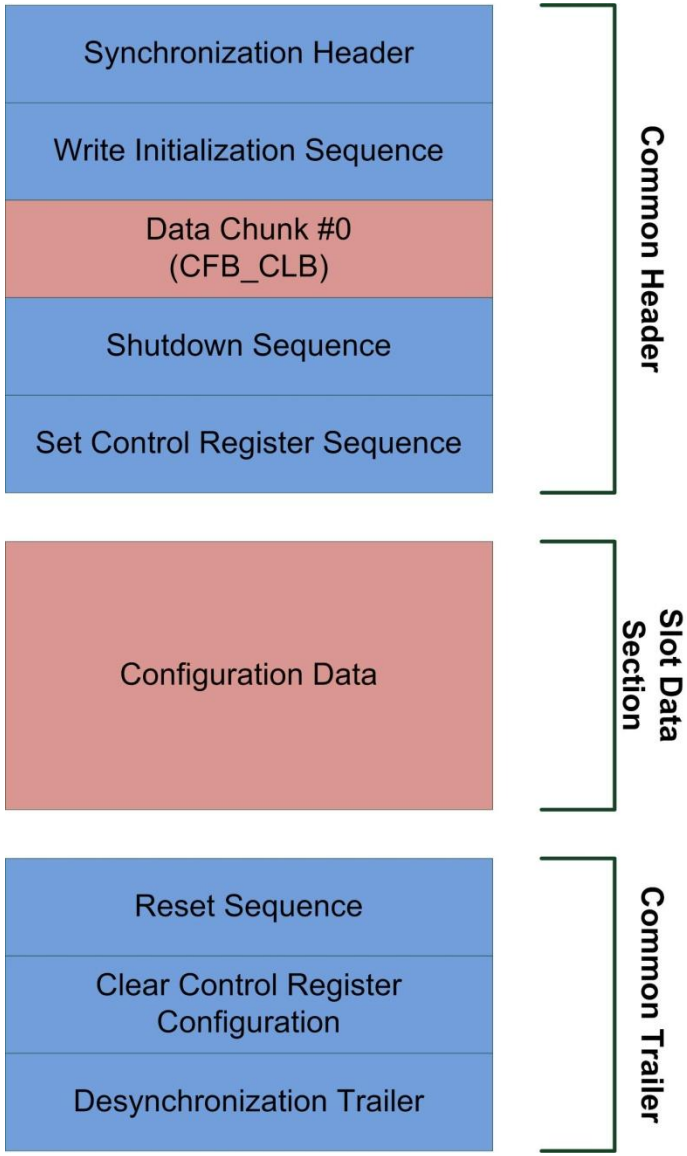


Valid Resumption Points

- Bitstream contain configuration data and commands.
- Commands control the Xilinx reconfiguration port (ICAP)
- The ABORT can be performed anywhere in the bitstream.
- Resumption point of reconfiguration must be carefully calculated.



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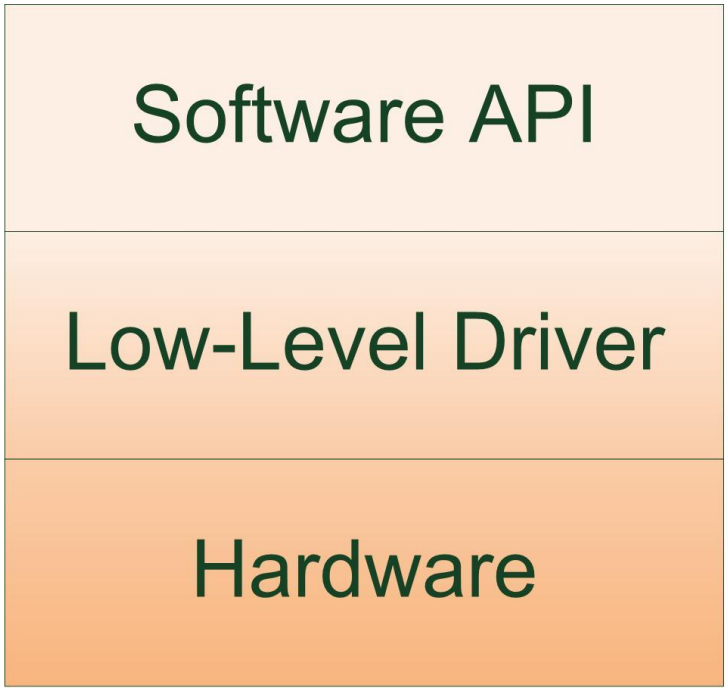
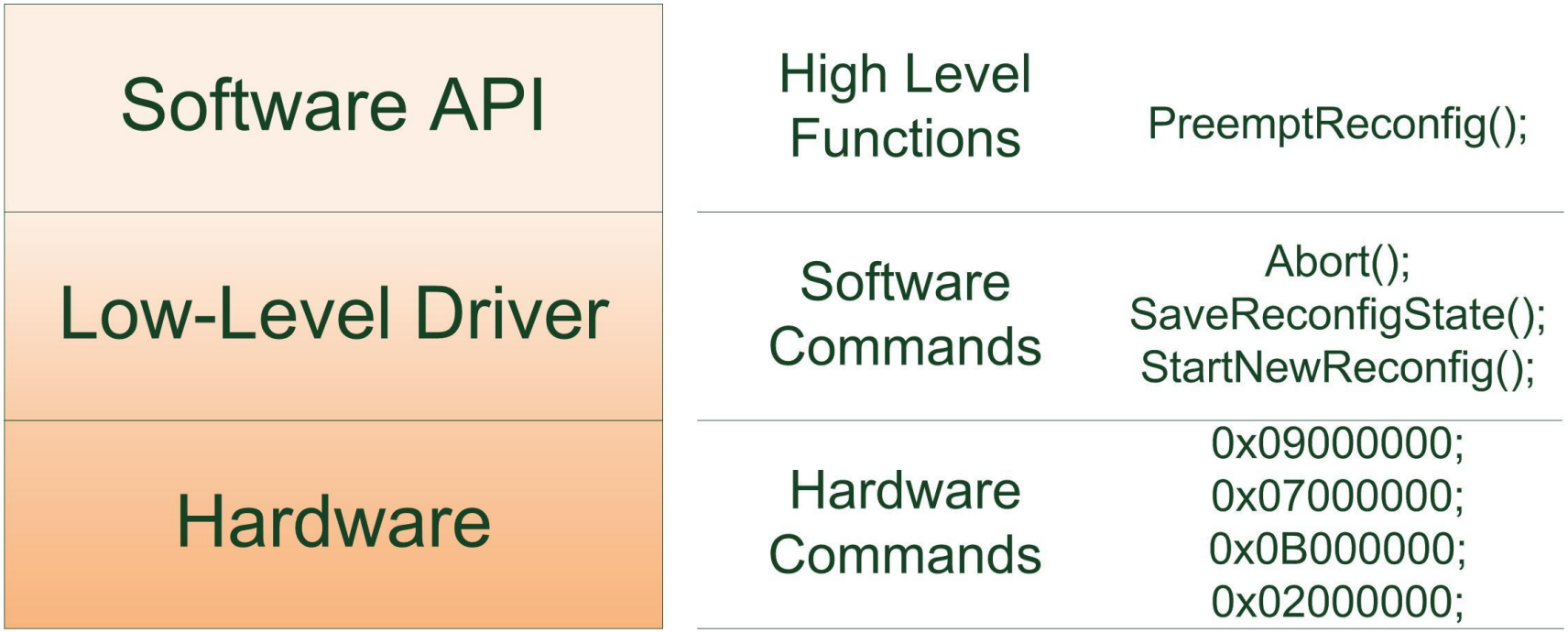


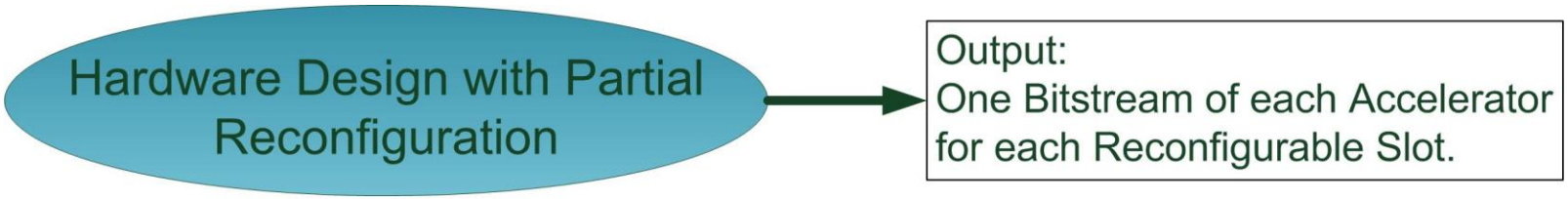
High Level Functions	PreemptReconfig();
Software Commands	Abort(); SaveReconfigState(); StartNewReconfig();
Hardware Commands	0x09000000; 0x07000000; 0x0B000000; 0x02000000;

Custom Reconfiguration Controller



- The hardware layer guarantees worst-case latency bounds on the commands it processes, even on the reconfiguration itself when a memory bandwidth is guaranteed.

Project Flow



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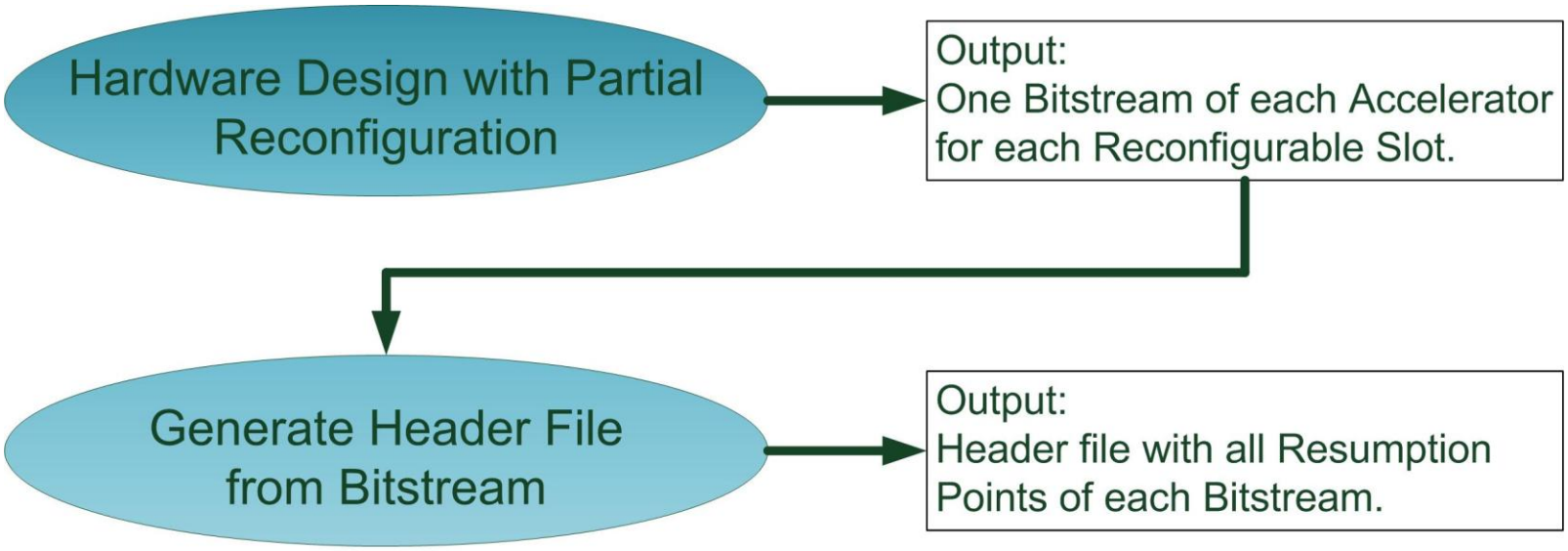

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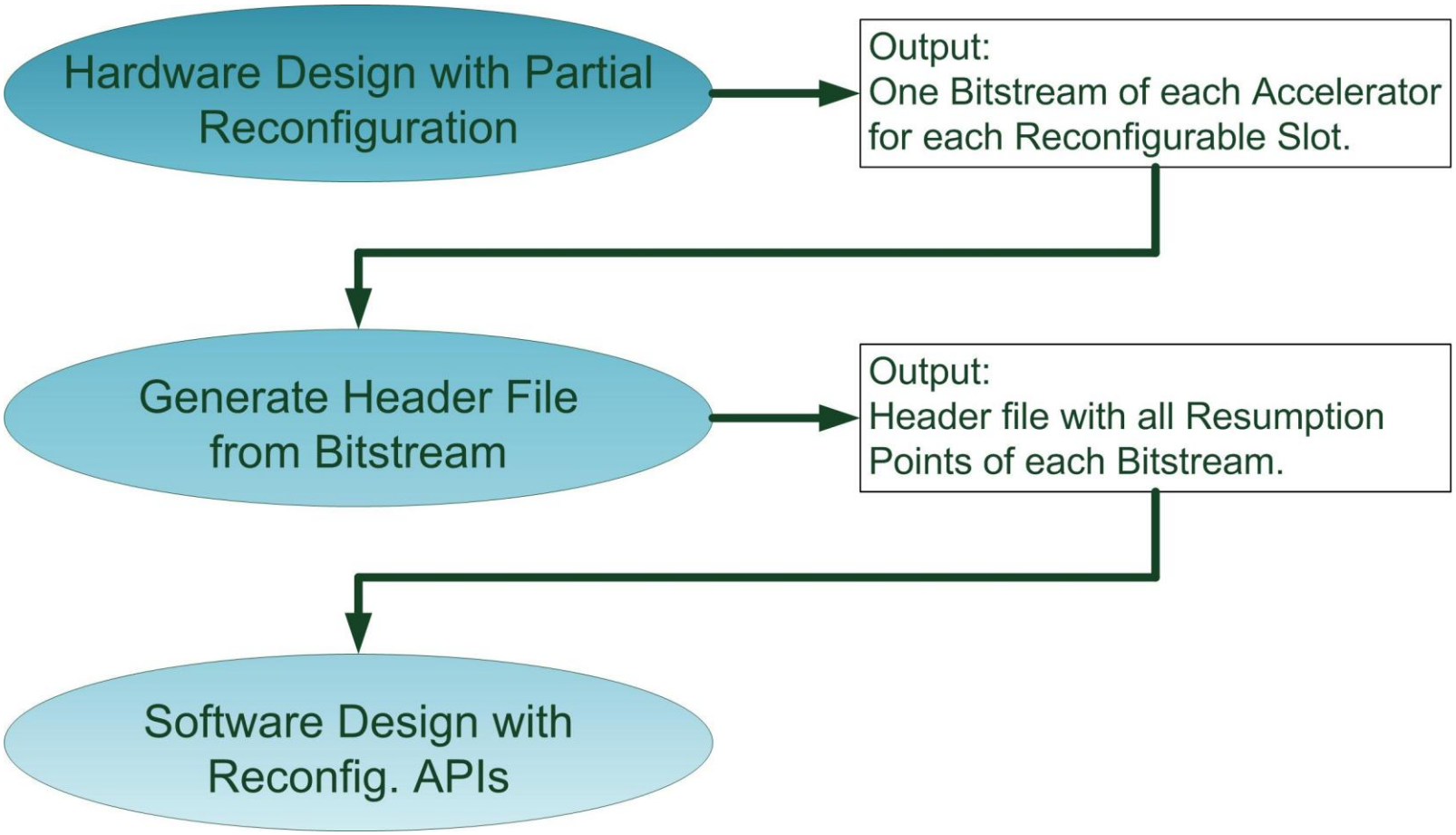

Measured Results

- High priority task
  - Period: from 5ms to 44ms (1ms step)
  - Reconfig. time: 0.79ms
- Low priority task
  - Period: 50ms
  - Reconfig. time: 32.63ms

	Low Priority Task		**High Priority Task**	
	Max. Observed Exec. Time	Avg. Observed Exec. Time	Max. Observed Exec. Time	Avg. Observed Exec. Time
No Abort	33.46 ms	32.68 ms	2.45 ms	0.805 ms
Abort	1664.12 ms	33.16 ms	0.811 ms	0.808 ms
Preemption	42.34 ms	32.68 ms	0.810 ms	0.805 ms

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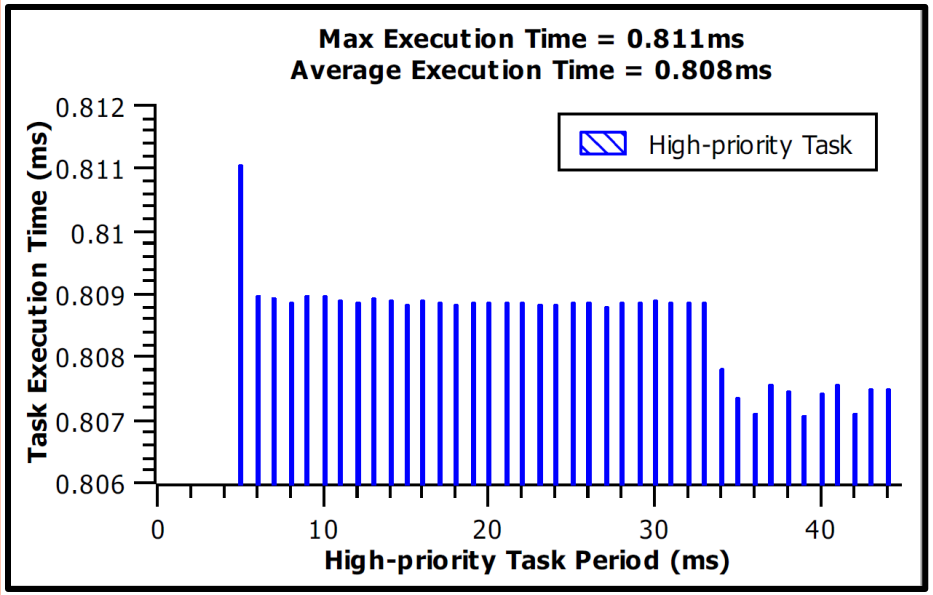
Starvation Experiment



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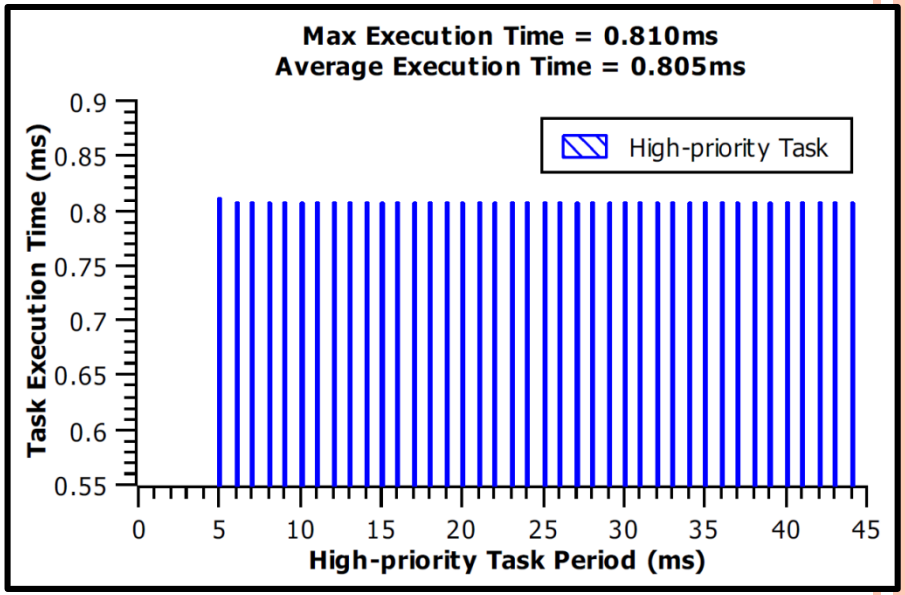

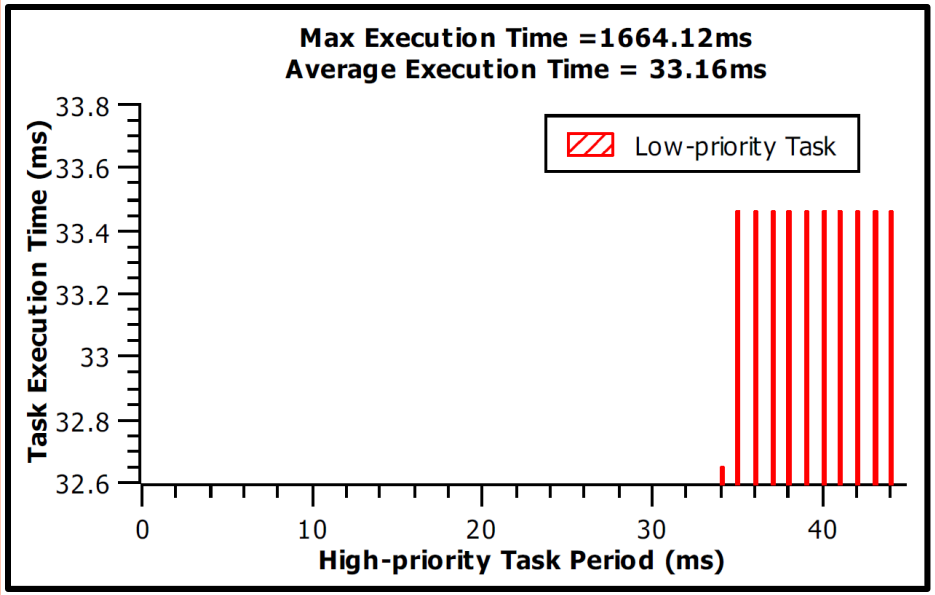

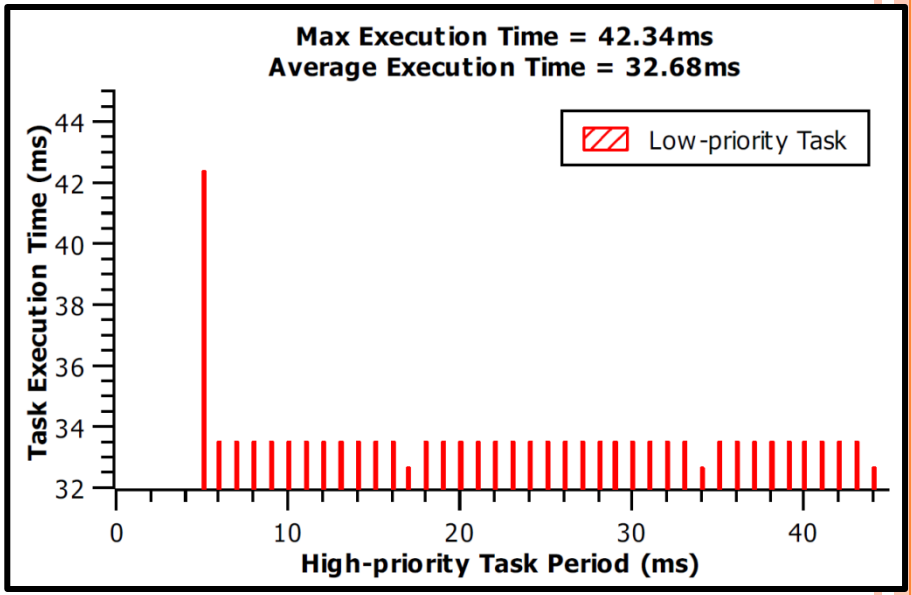

Conclusions

- Design and realization of Preemptable Reconfiguration with guaranteed latencies
  - Custom Reconfiguration Controller
  - Software driver, API
  - Tools to analyze and manipulate bitstreams
- Base application developed on a RealTime OS (FreeRTOS) that benefits from having Preemptable Reconfiguration


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