2nd Italian Workshop on Embedded Systems

IWES 2017

Dynamic Trade-Off Management for CPS

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7-8 September 2017 – Rome (IT)

Outline

- Introduction
  - CERBERO and Cyber Physical Systems
  - HEVC Codec and Software Approximate Computing
- Approximate HEVC interpolators
  - Coarse-Grained Reconfiguration
  - From CG HEVC Interpolators to CGR HEVC Interpolators
- Results
  - Achieved Adaptivity
  - Comparison with the State of the Art
- Conclusions

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CERBERO project

Cross-layer mod**E**l-based framewo**R**k for multi-o**B**jective d**E**sign of **R**econfigurable systems in unce**R**tain hyb**R**id envir**O**nments

→ continuous design environment for **Cyber-Physical Systems (CPS)** including modelling, deployment and verification

http://www.cerbero-h2020.eu/

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Cyber Physical Systems (CPS)

Complex systems with **different interacting and deeply intertwined components**, providing multiple and distinct **behavioral modalities** potentially **changing over time**, that contribute **concurrently** to determine the behavior of the system as a whole.

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Layers (dominat aspects):

- functional
- physical
- communication

Subjected to **Functional** (F) and **Non-Functional** (NF) requirements variation in time.

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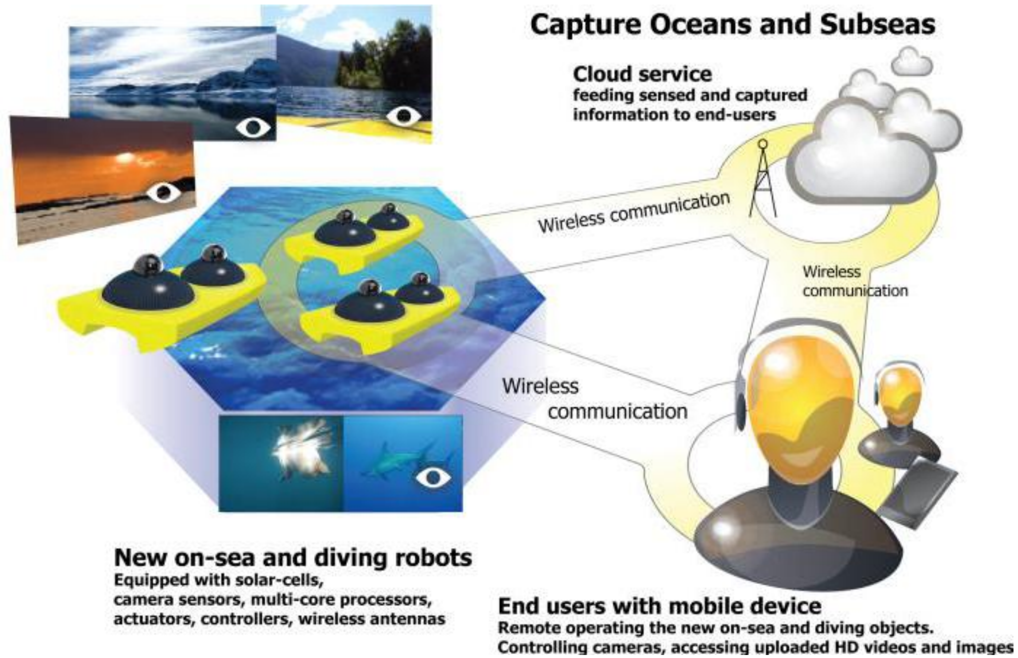
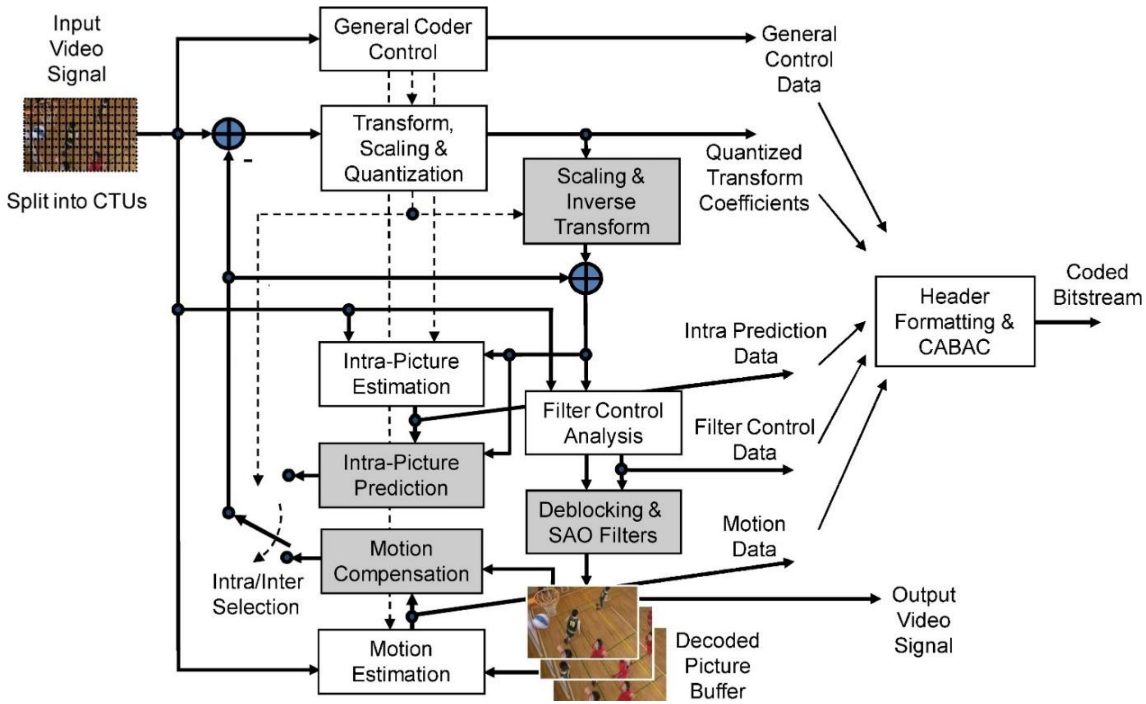


High Efficiency Video Coding (HEVC)

Recent video codec developed by the Joint Collaboration Team on Video Coding (VCEG and MPEG). It provides up to **50% bit rate reduction at the same subjective video quality** with respect to previous standards (H.264).



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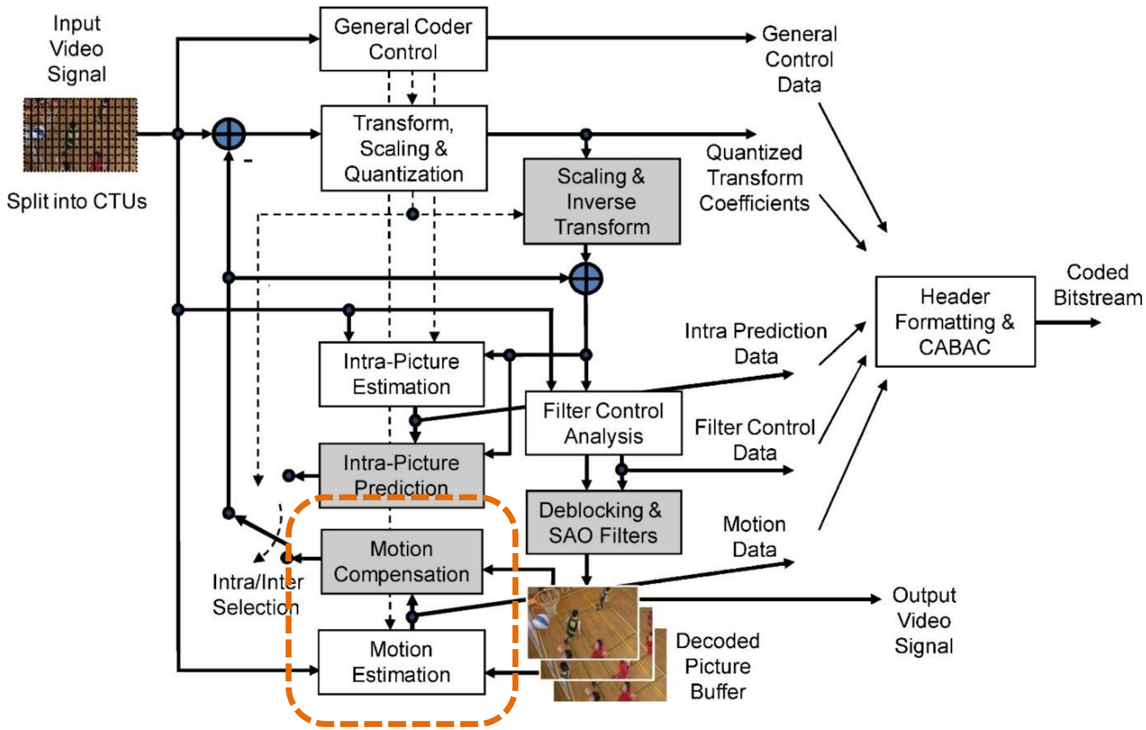

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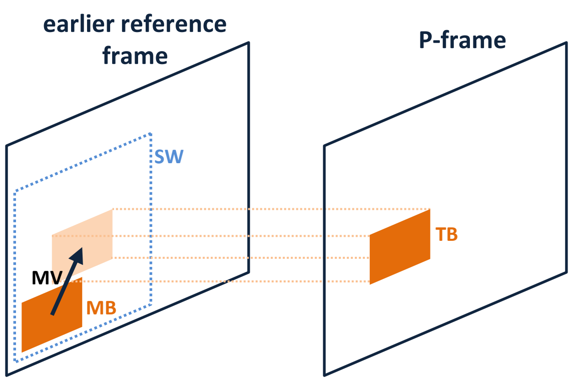
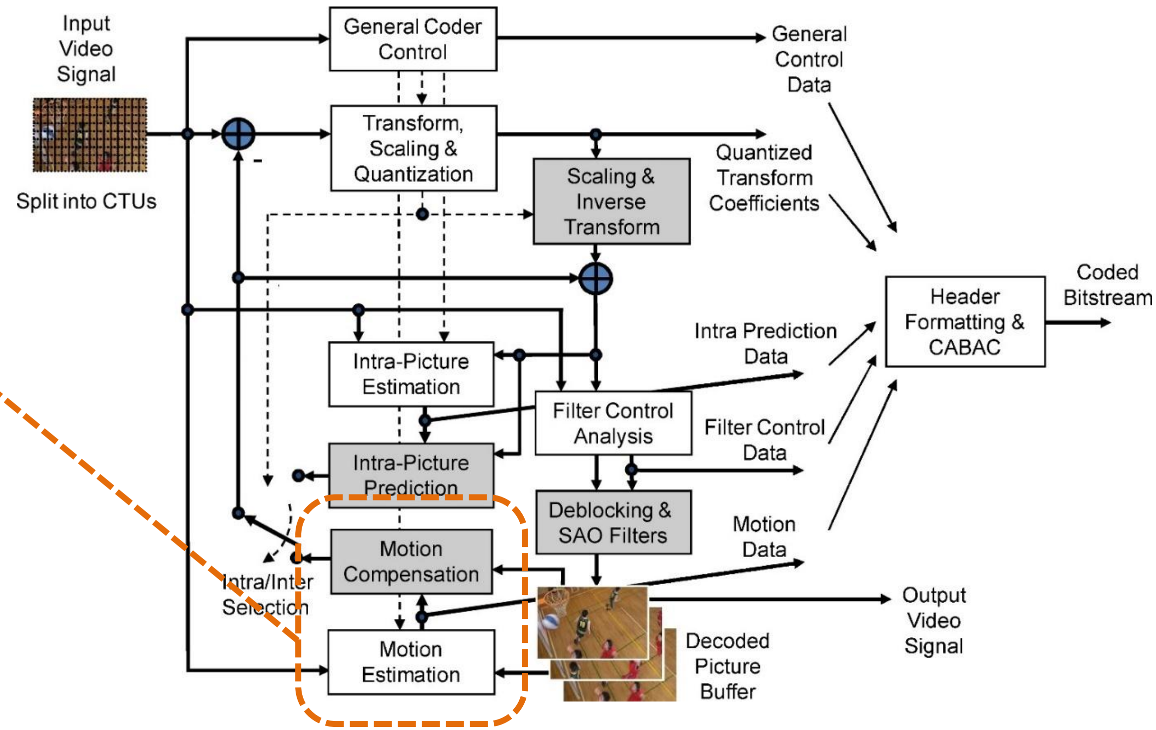
Computational Intensive and Power Hungry Step: Motion Estimation and Compensation



TB = target block
MB = matching block
SW = search window
MV = motion vector



Approximate HEVC Interpolation in Software

With high frame rates the **motion vector** could be composed of **fractional pixel** values. In these cases an **interpolation (FIR filtering)** of the matching block is necessary.

		1/4	1/2	3/4	
	A_{00}	a_{00}	b_{00}	c_{00}	A_{01}
1/4	d_{00}	e_{00}	f_{00}	g_{00}	
1/2	h_{00}	i_{00}	l_{00}	m_{00}	
3/4	n_{00}	o_{00}	p_{00}	q_{00}	
	A_{10}				A_{11}

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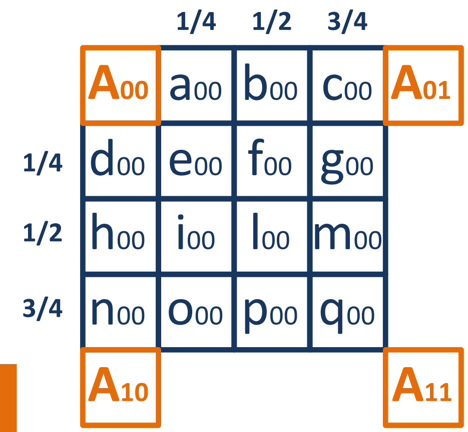

luma MV α	legacy	approximate [1]			
	8/7 tap	7 tap	5 tap	3 tap	1 tap
1/4, 3/4	-1, 4, -10, 58, 17, -5, 1	-1, 4, -10, 58, 17, -5, 1	1, -6, 20, 54, -5	-4, 20, 48	64
1/2	-1, 4, -11, 40, 40, -11, 4, -1	-1, 4, 11, 40, 40, -11, 3	2, -9, 40, 40, -9	-9, 41, 32	64

chroma MV α	legacy	approximate [1]		
	4 tap	3 tap	2 tap	1 tap
1/8, 7/8	-2, 58, 10, -2	-3, 62, 5	58, 7	64
1/4, 3/4	-4, 54, 16, -2	-5, 58, 11	50, 15	64
3/8, 5/8	-6, 46, 28, -4	-7, 51, 20	41, 23	64
1/2	-4, 36, 36, -4	-6, 42, 28	32, 32	64

[1] *E. Nogues et al., "Algorithmic-level approximate computing applied to energy efficient hevc decoding," IEEE Trans. On Emerging Topics in Computing, 2016.*

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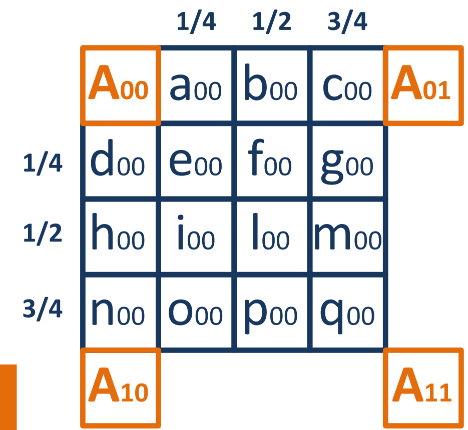

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1/2	-1, 4, -11, 40, 40, -11, 4, -1	-1, 4, 11, 40, 40, -11, 3	2, -9, 40, 40, -9	-9, 41, 32	64

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→ up to **28% energy saving** with a **small degradation** of decoding quality on an ARM big.LITTLE SoC

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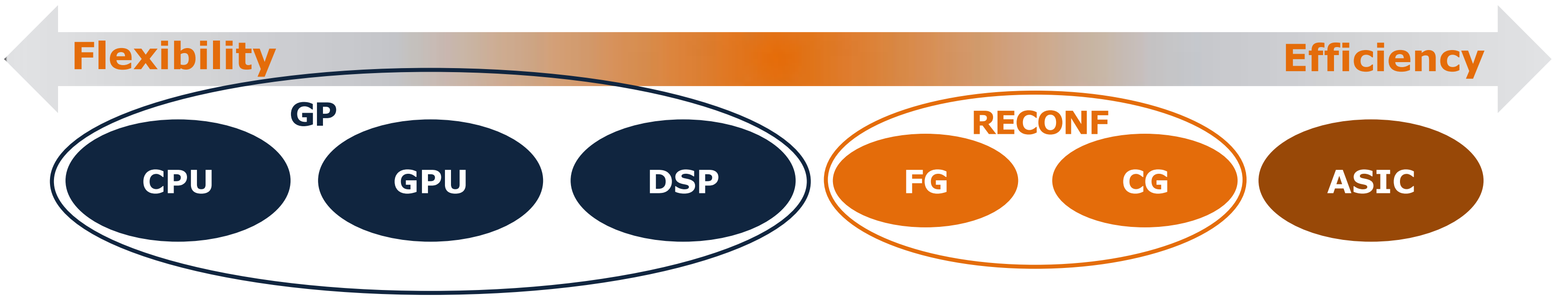
Coarse-Grained Reconfiguration (CGR)



Reconfigurable computing provides a **trade-off between execution efficiency** typical of ASICs **and flexibility** mainly exhibited by GP devices.

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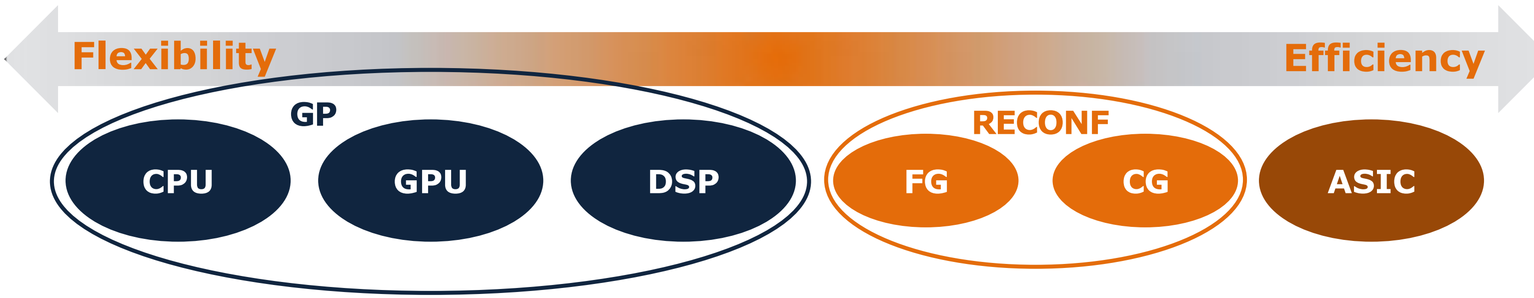
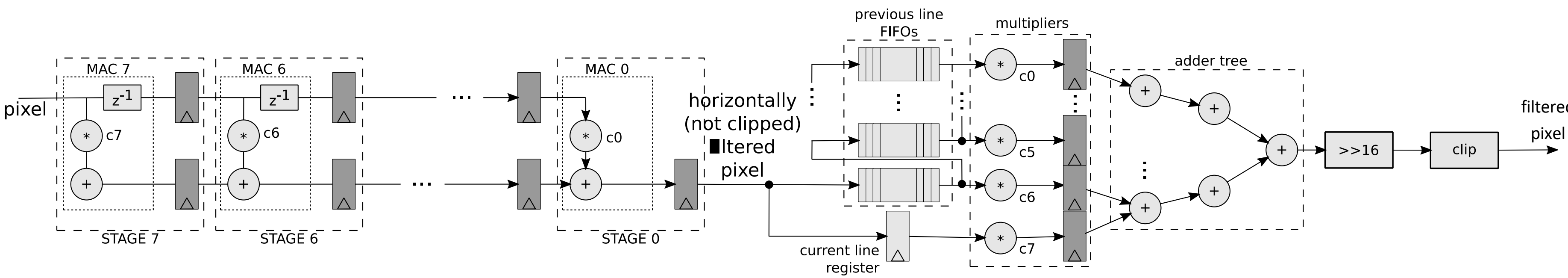


Reconfigurable computing provides a **trade-off between execution efficiency** typical of ASICs **and flexibility** mainly exhibited by GP devices.

	Fine-Grained (FG) bit-level	Coarse-Grained (CG) word-level
flexibility	☺	😐
speed	😐	☺
memory	☹	😐

CG HEVC interpolators



example N=4

X_{8x8}

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55
56	57	58	59	60	61	62	63

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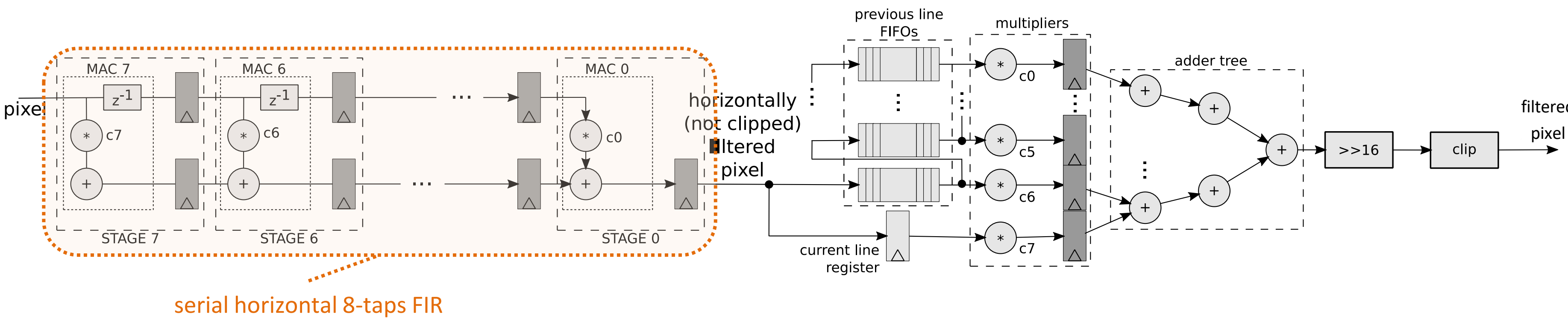

example N=4

y3=c0x2+c1x3+c2x4+c3x5

y2=c0x1+c1x2+c2x3+c3x4

y1=c0x0+c1x1+c2x2+c3x3

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24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
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→ horizontal Filtering (N-1 cols)

Y_{8x5}

-	1	2	3	4	5	-	-
-	9	10	11	12	13	-	-
-	17	18	19	20	21	-	-
-	25	26	27	28	29	-	-
-	33	34	35	36	37	-	-
-	41	42	43	44	45	-	-
-	49	50	51	52	53	-	-
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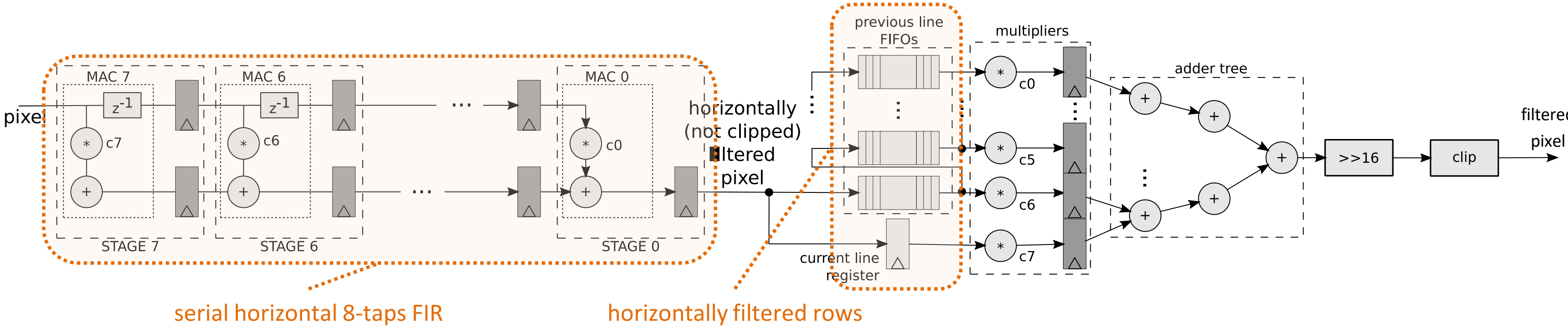

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-	33	34	35	36	37	-	-
-	41	42	43	44	45	-	-
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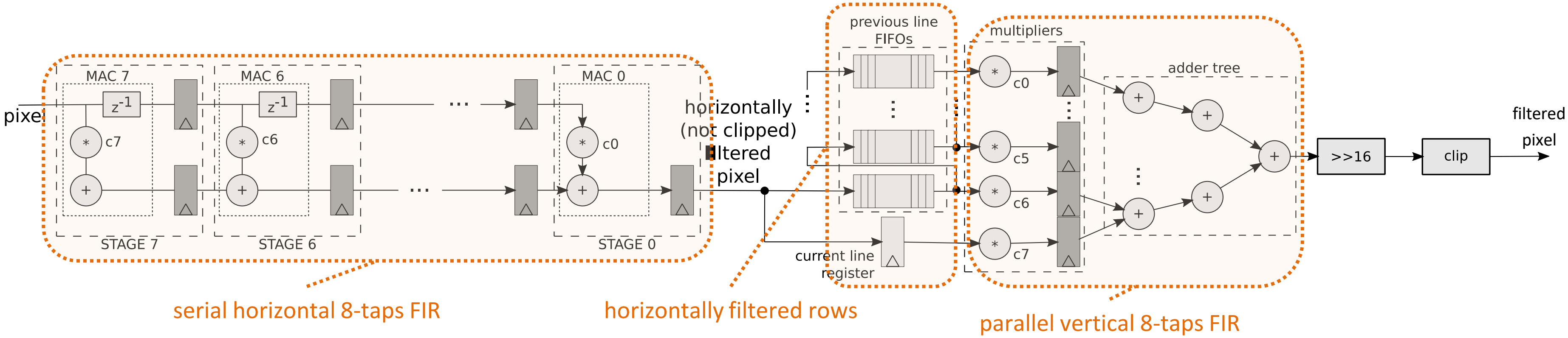

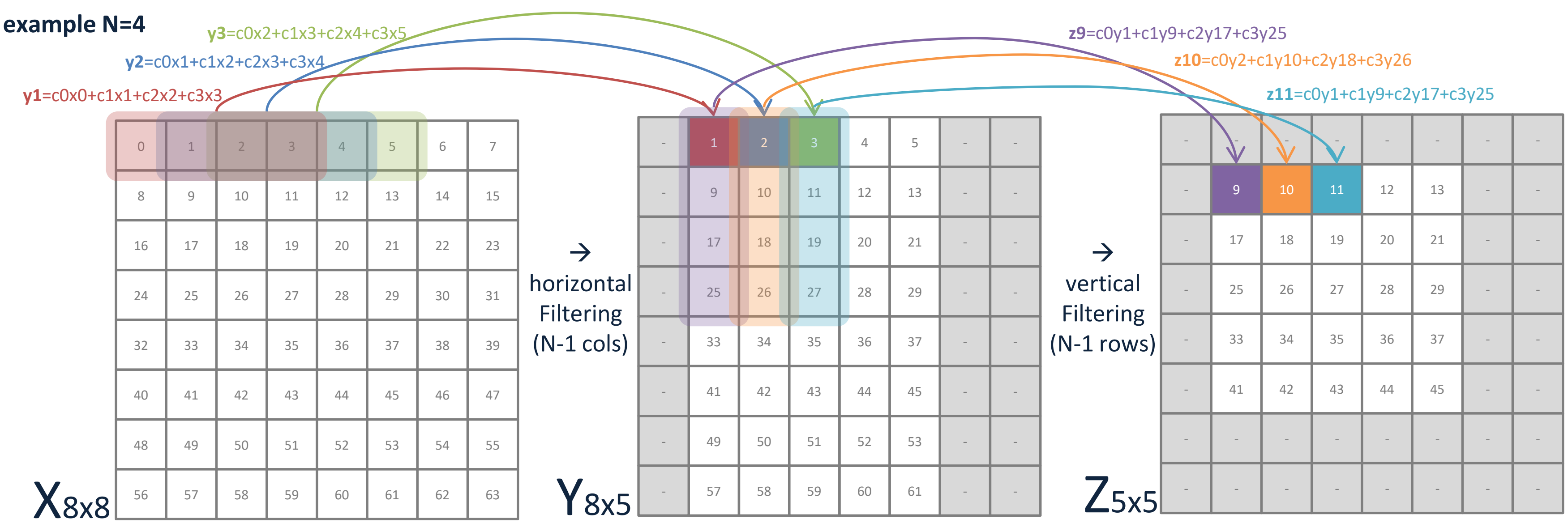

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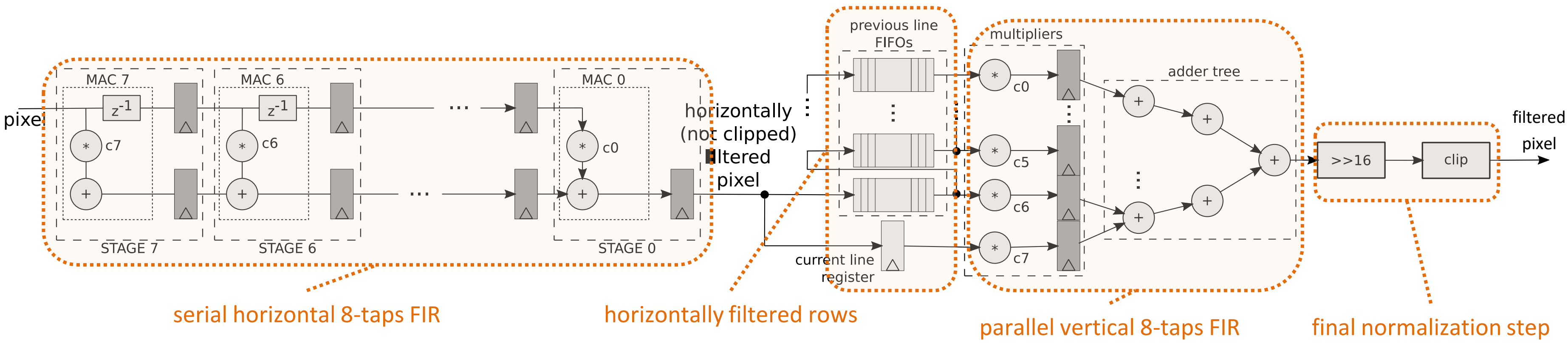
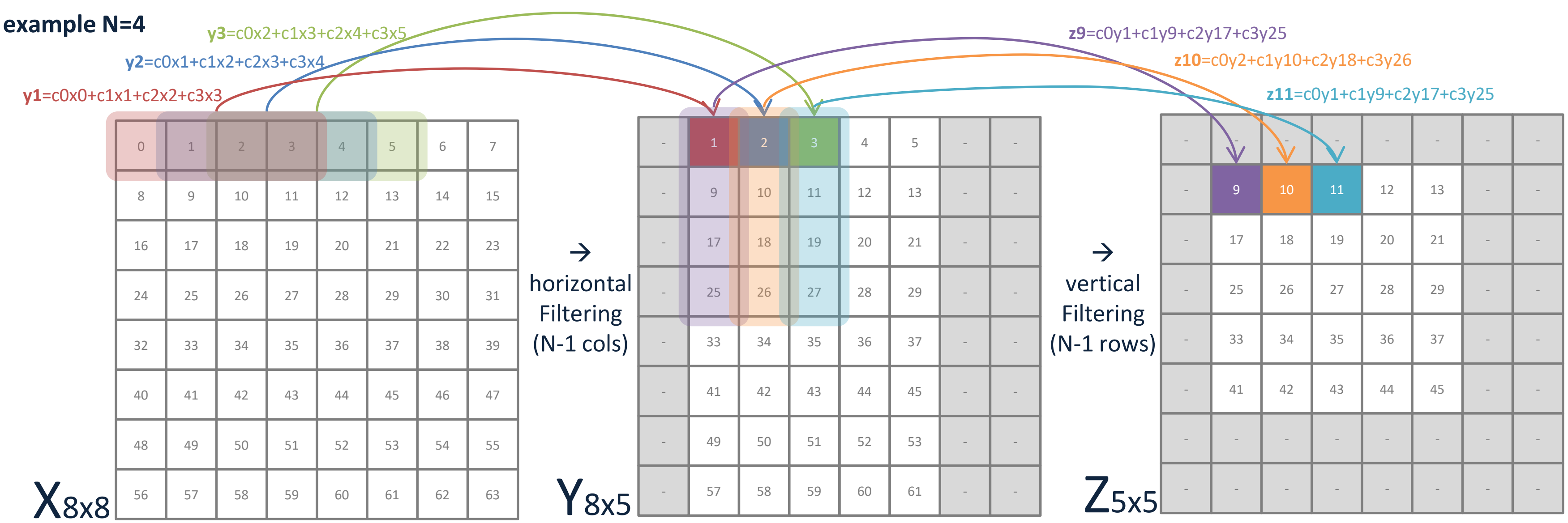
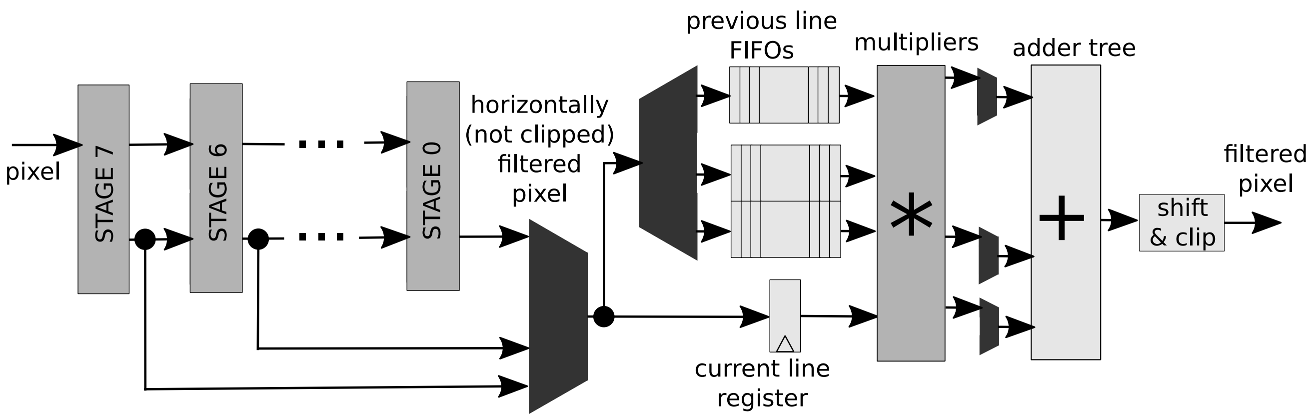




CGR HEVC interpolators



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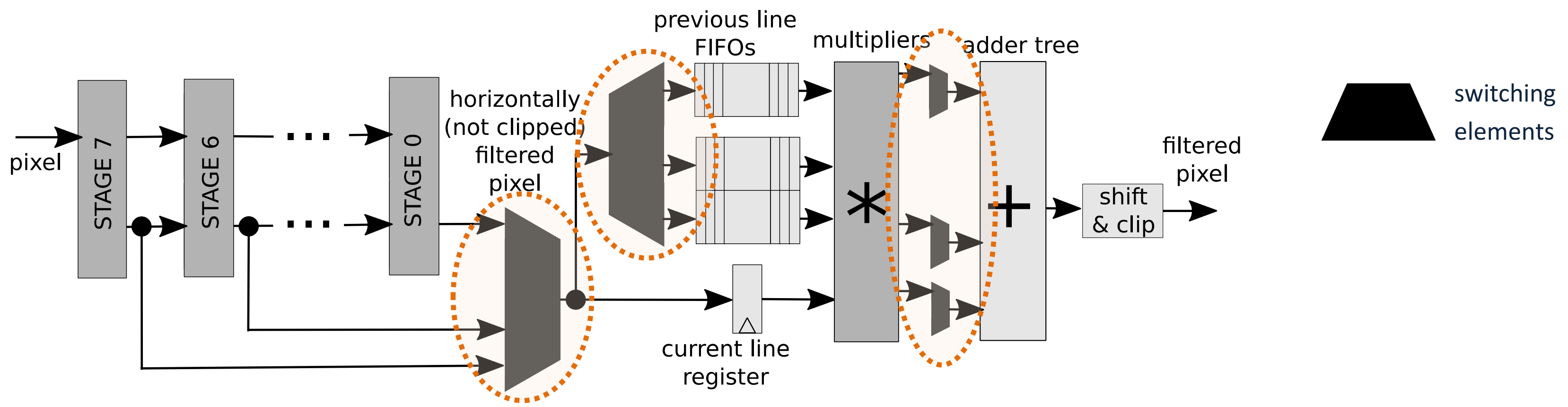

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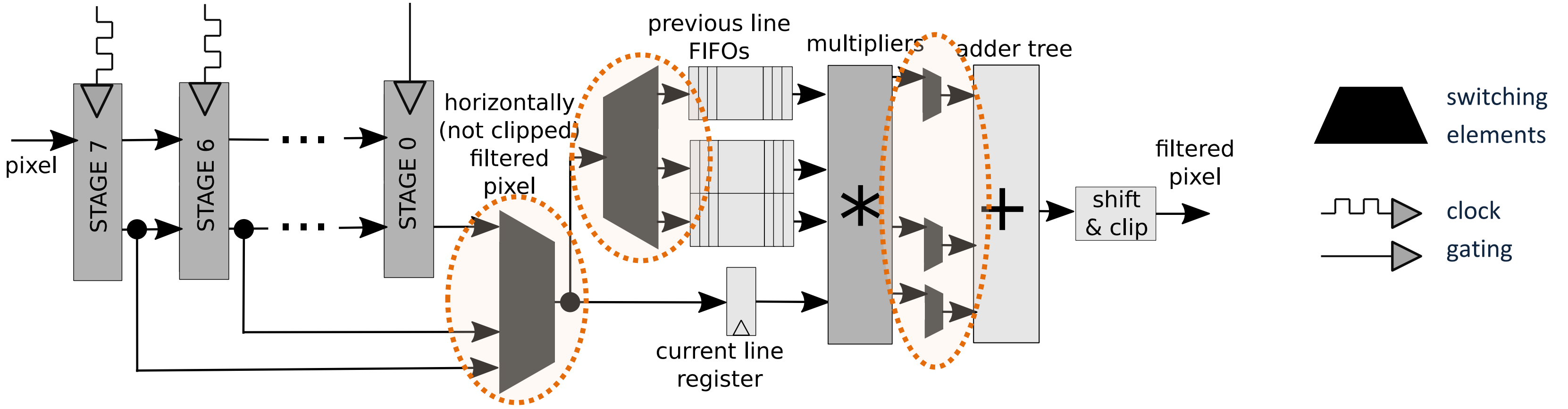

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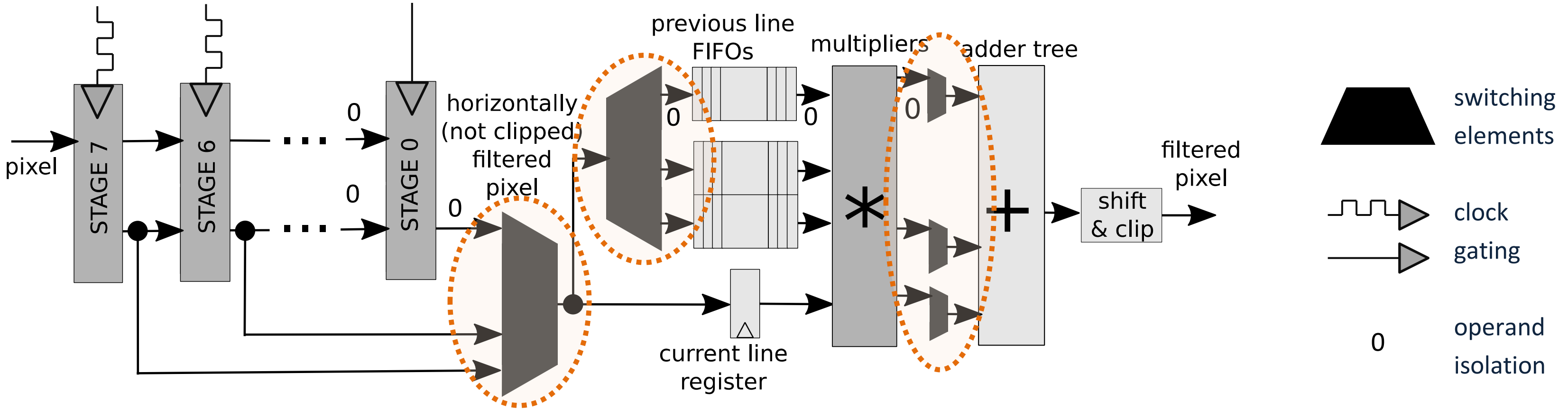

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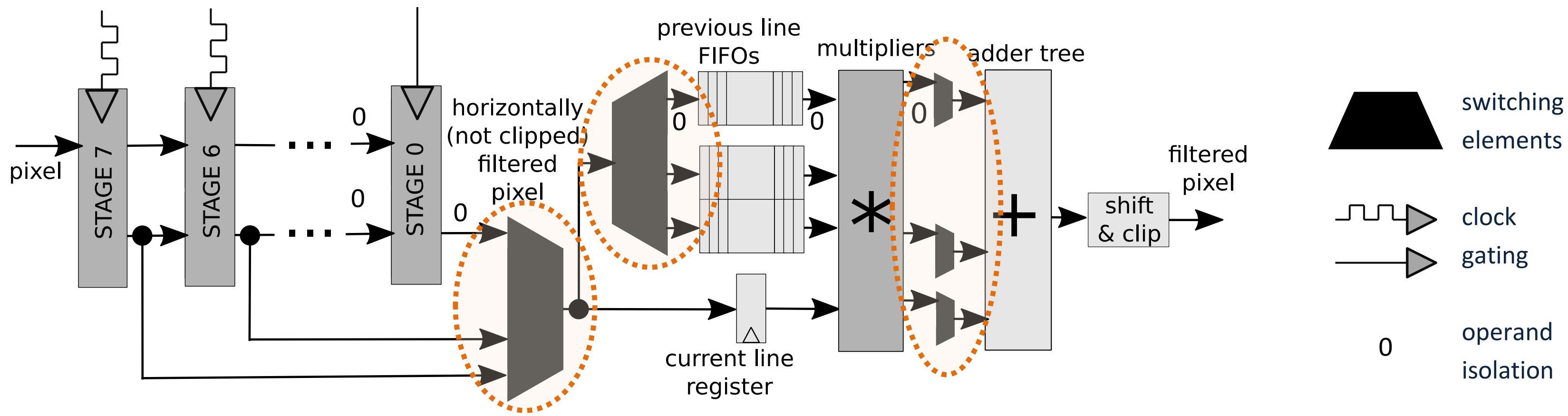

profile	HIGH		
	quality	# taps	energy
luma	☺	8/7	☹
chroma		4	

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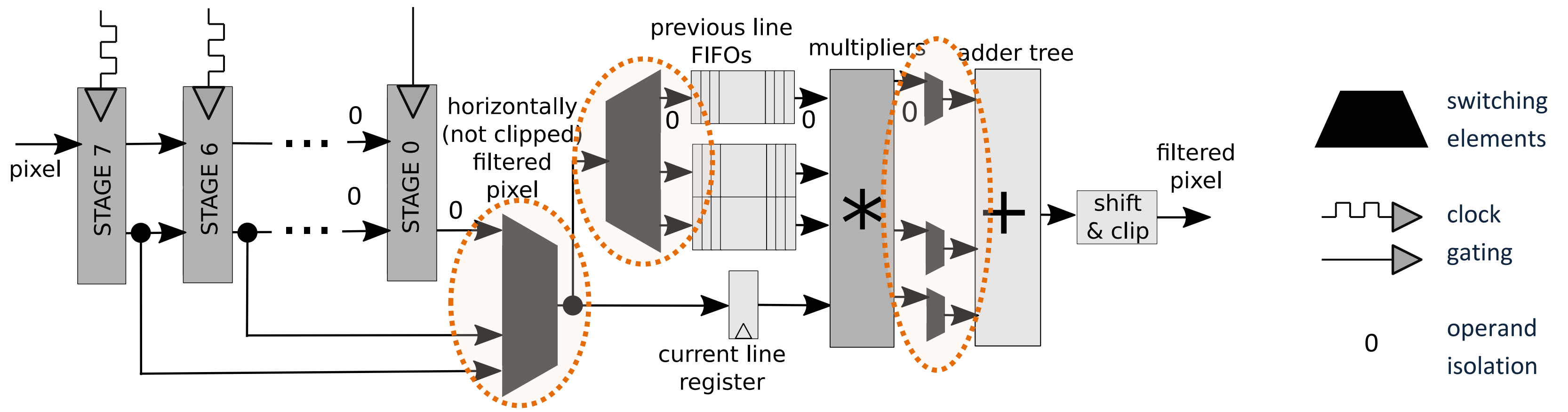

profile	HIGH			MEDIUM		
	quality	# taps	energy	quality	# taps	energy
luma	☺	8/7	☹	😐	5	😐
chroma		4			3	

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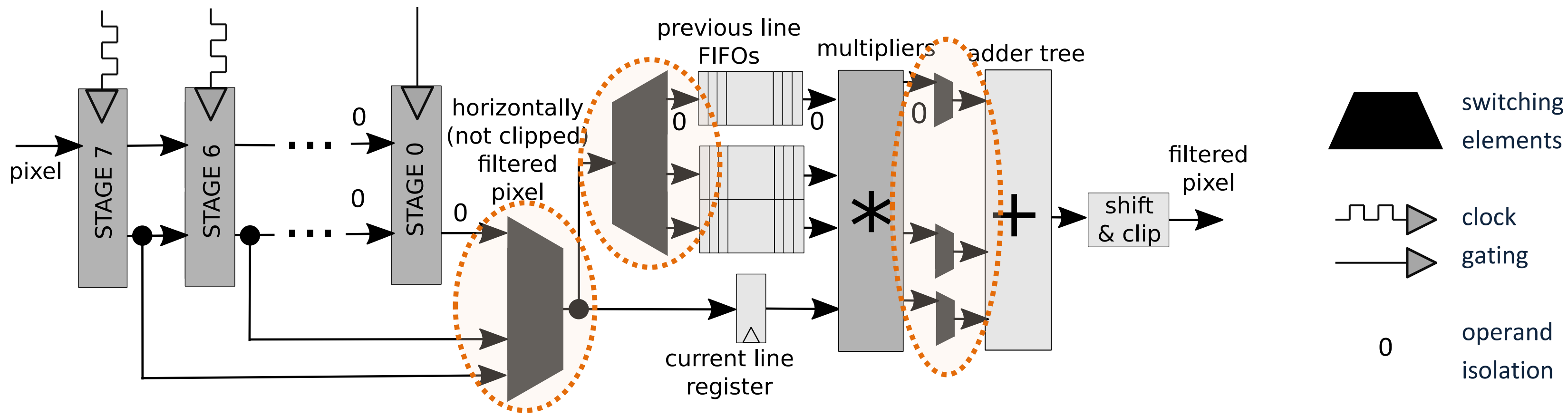

profile	HIGH			MEDIUM			LOW		
	quality	# taps	energy	quality	# taps	energy	quality	# taps	energy
luma	☺	8/7	☹	😐	5	😐	☹	3	☺
chroma		4			3			2	

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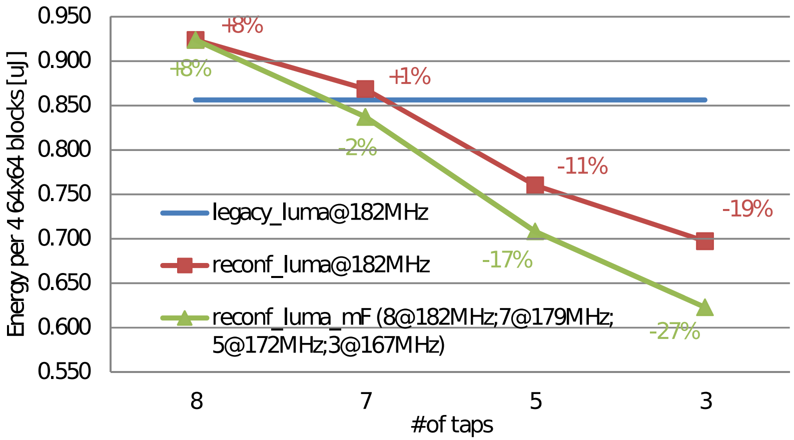
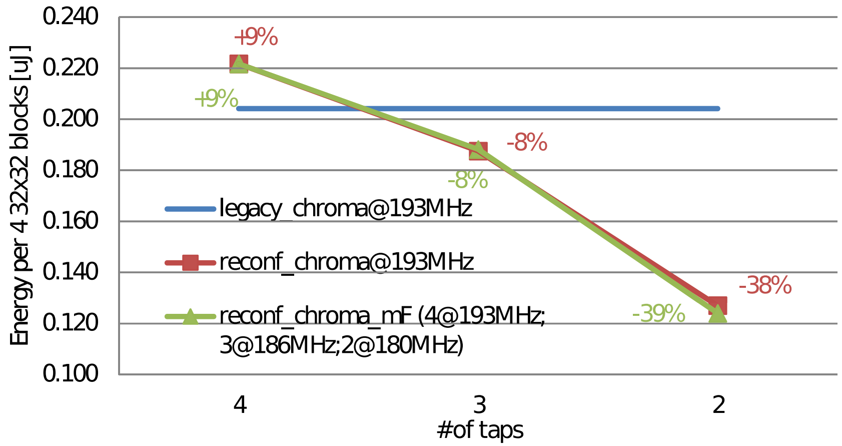
Achieved Adaptivity

design @200 MHz Xilinx XC7Z020	LUT	FF	BRAM	DSP	Fmax [MHz]	tap	dP (Vivado) [mW]	dE [µJ]	time per block [cycles]	# interpolated pixels in a fixed time
legacy_luma	212	37	4	16	213	8	11	0.248	460	57957
reconf_luma (vs legacy %)	582 (+175%)	85 (+130%)	4 (+0%)	16 (+0%)	200 (-6%)	8	12 (+9%)	0.270 (+9%)	460 (+0%)	57957 (+0%)
						7	11 (+0%)	0.245 (-1%)	395 (-14%)	59033 (+2%)
						5	10 (-9%)	0.217 (-12%)	265 (-42%)	61191 (+6%)
						3	10 **(-9%)**	0.211 **(-15%)**	135 **(-71%)**	63357 **(+9%)**
legacy_chroma	163	33	2	8	217	4	9	0.053	107	14753
reconf_chroma (vs legacy %)	383 (+135%)	65 (+97%)	2 (+0%)	8 (+0%)	200 (-12%)	4	9 (+0%)	0.053 (+0%)	107 (+0%)	14753 (+0%)
						3	8 (-11%)	0.045 (-13%)	73 (-32%)	15293 (+4%)
						2	6 **(-33%)**	0.033 **(-37%)**	39 **(-64%)**	15835 **(+7%)**





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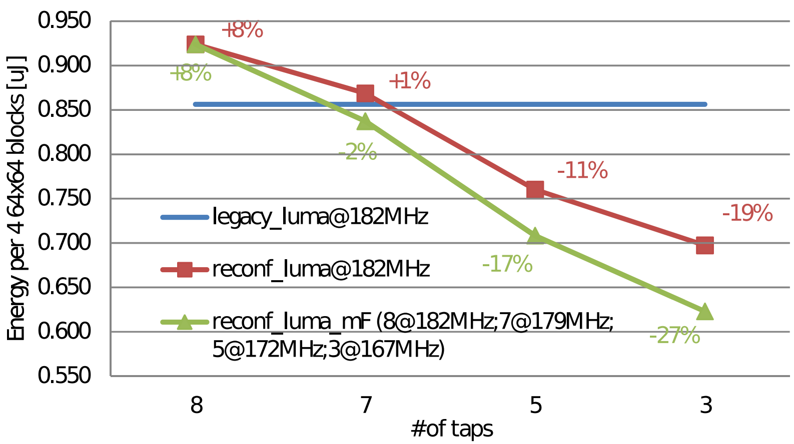

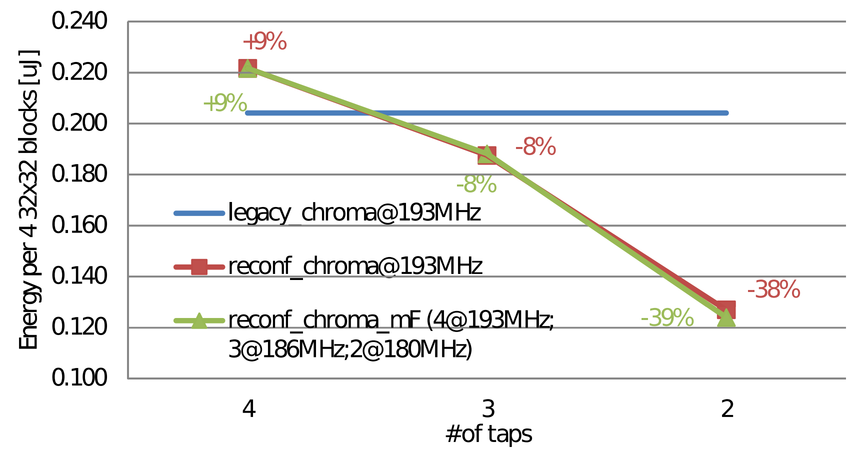

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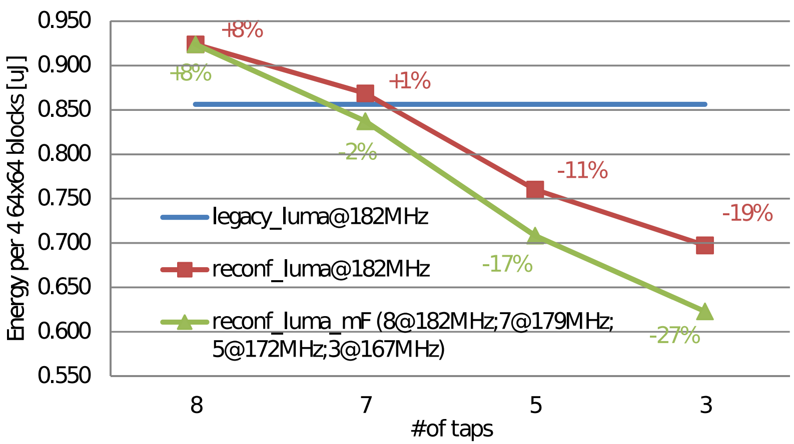
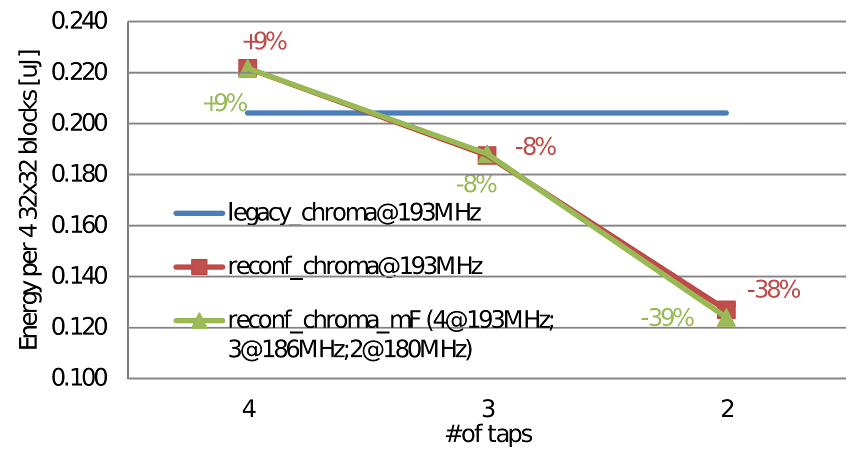
						2	6 **(-33%)**	0.033 **(-37%)**	39 **(-64%)**	15835 **(+7%)**





Achieved Adaptivity

design @200 MHz Xilinx XC7Z020	LUT	FF	BRAM	DSP	Fmax [MHz]	tap	dP (Vivado) [mW]	dE [μJ]	time per block [cycles]	# interpolated pixels in a fixed time
legacy_luma	212	37	4	16	213	8	11	0.248	460	57957
reconf_luma (vs legacy %)	582 (+175%)	85 (+130%)	4 (+0%)	16 (+0%)	200 (-6%)	8	12 (+9%)	0.270 (+9%)	460 (+0%)	57957 (+0%)
						7	11 (+0%)	0.245 (-1%)	395 (-14%)	59033 (+2%)
						5	10 (-9%)	0.217 (-12%)	265 (-42%)	61191 (+6%)
						3	10 **(-9%)**	0.211 **(-15%)**	135 **(-71%)**	63357 **(+9%)**
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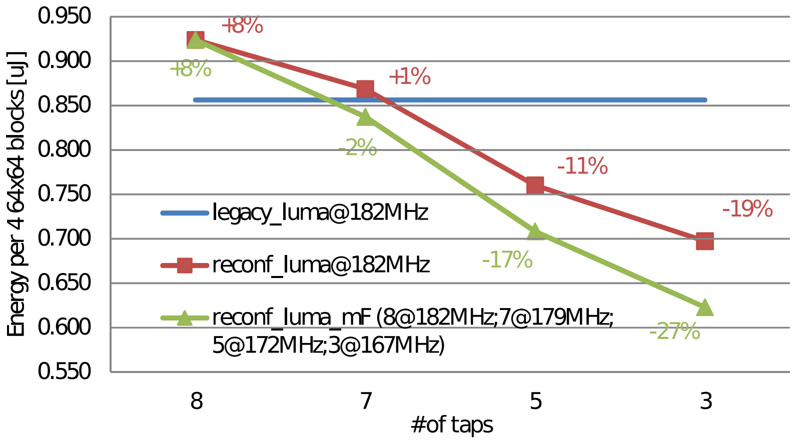

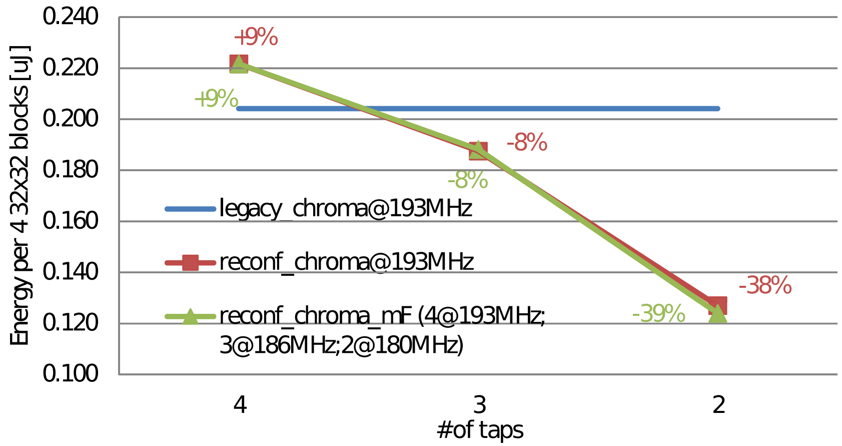

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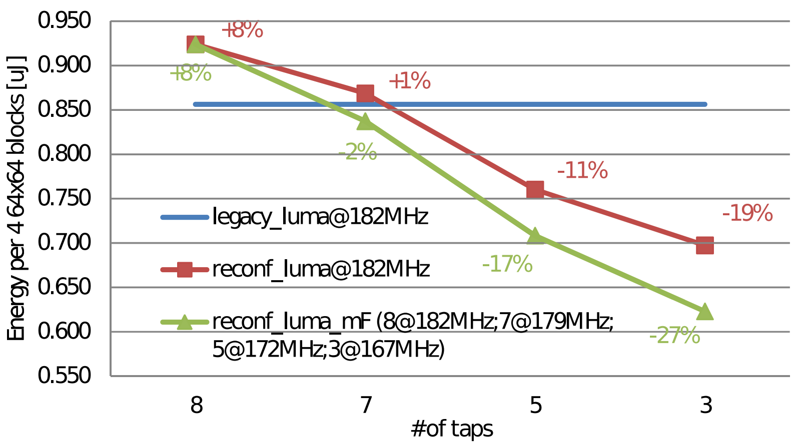
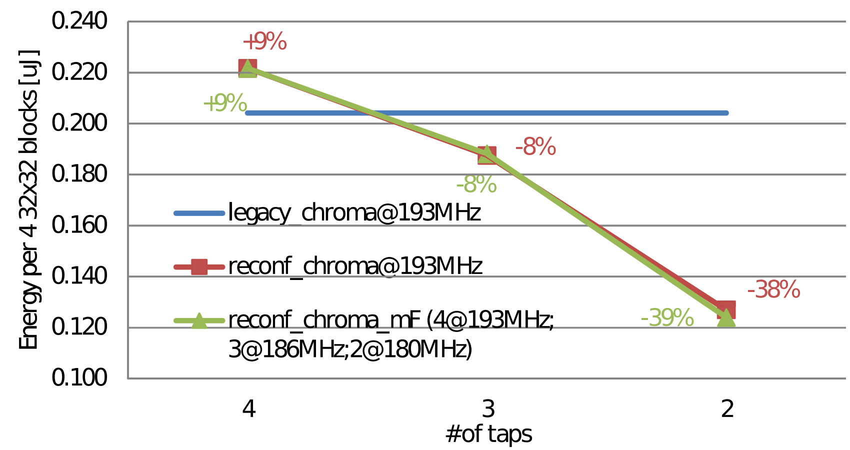
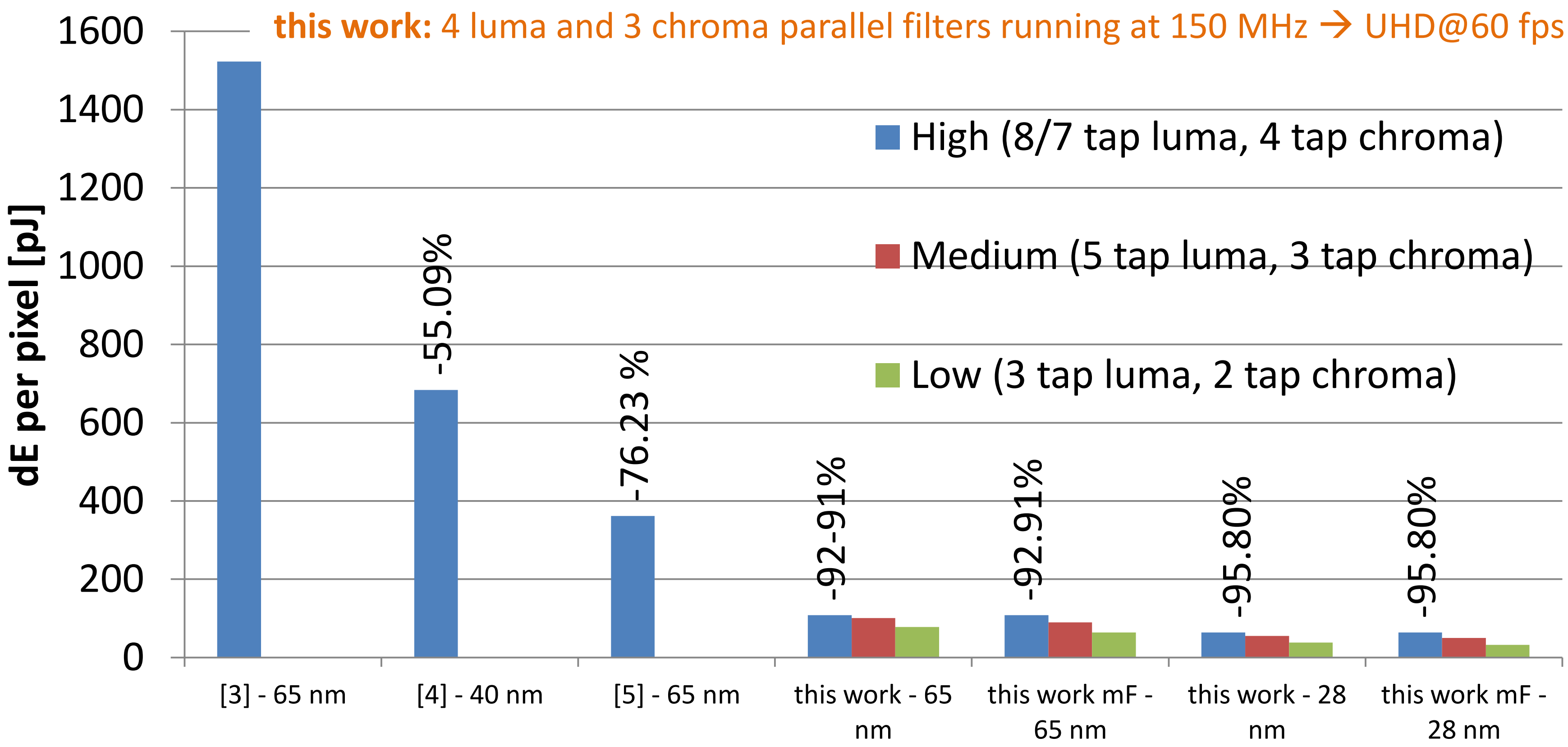




Comparison with the State of the Art



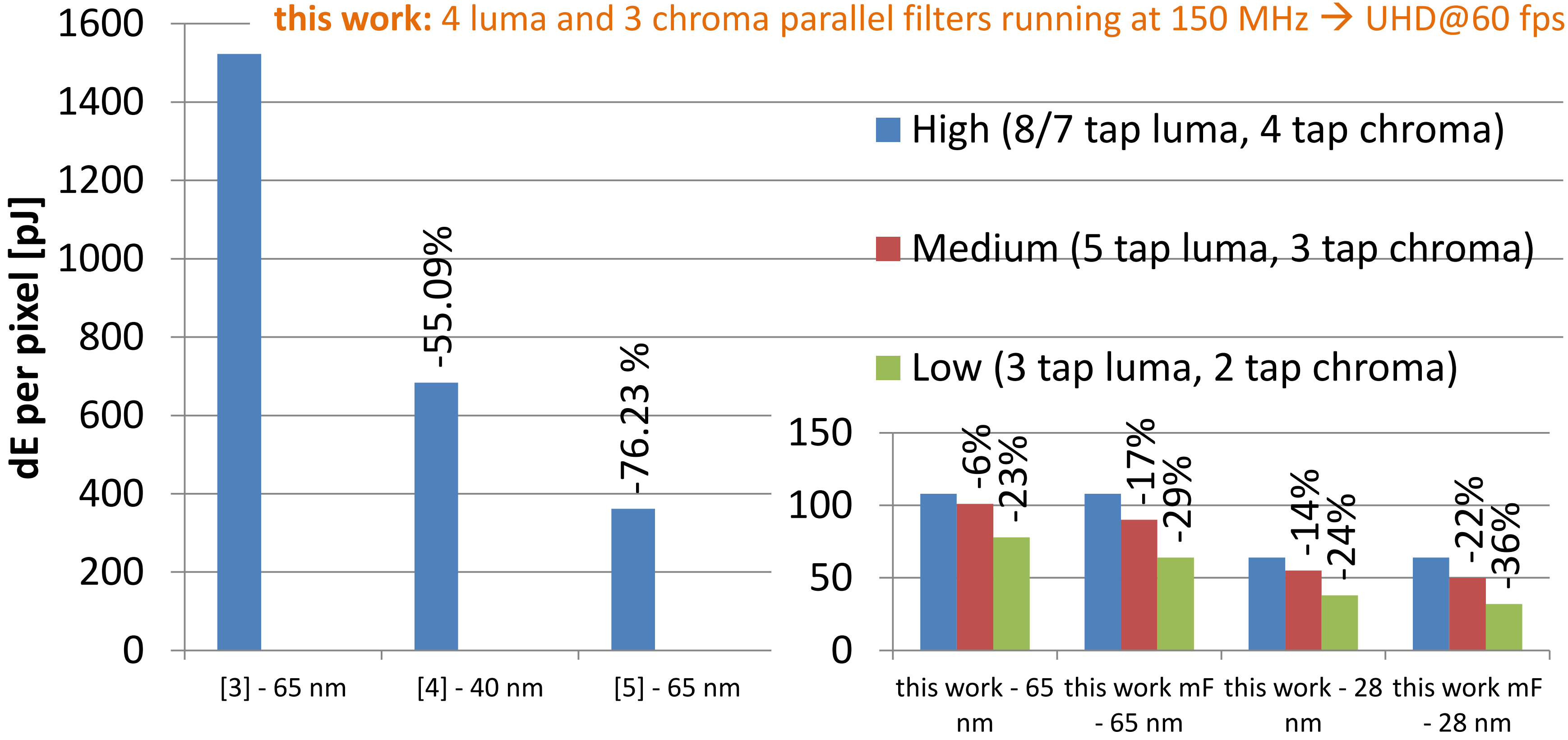
[3] V. Afonso et al., "Low cost and high throughput FME interpolation for the HEVC emerging video coding standard," Proc. of the IEEE LASCAS Conf., 2013.

[4] E. Kalali et al., "A reconfigurable HEVC sub pixel interpolation hardware," Proc. of the IEEE ICCE Conf., 2013.

[5] C. M. Diniz et al., "A reconfigurable hardware architecture for fractional pixel interpolation in high efficiency video coding," IEEE Comput.-Aided Des. Integr. Circuits Syst., vol. 34, no. 2, pp. 238–251, 2015.

Comparison with the State of the Art

this work: 4 luma and 3 chroma parallel filters running at 150 MHz → UHD@60 fps



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Outline

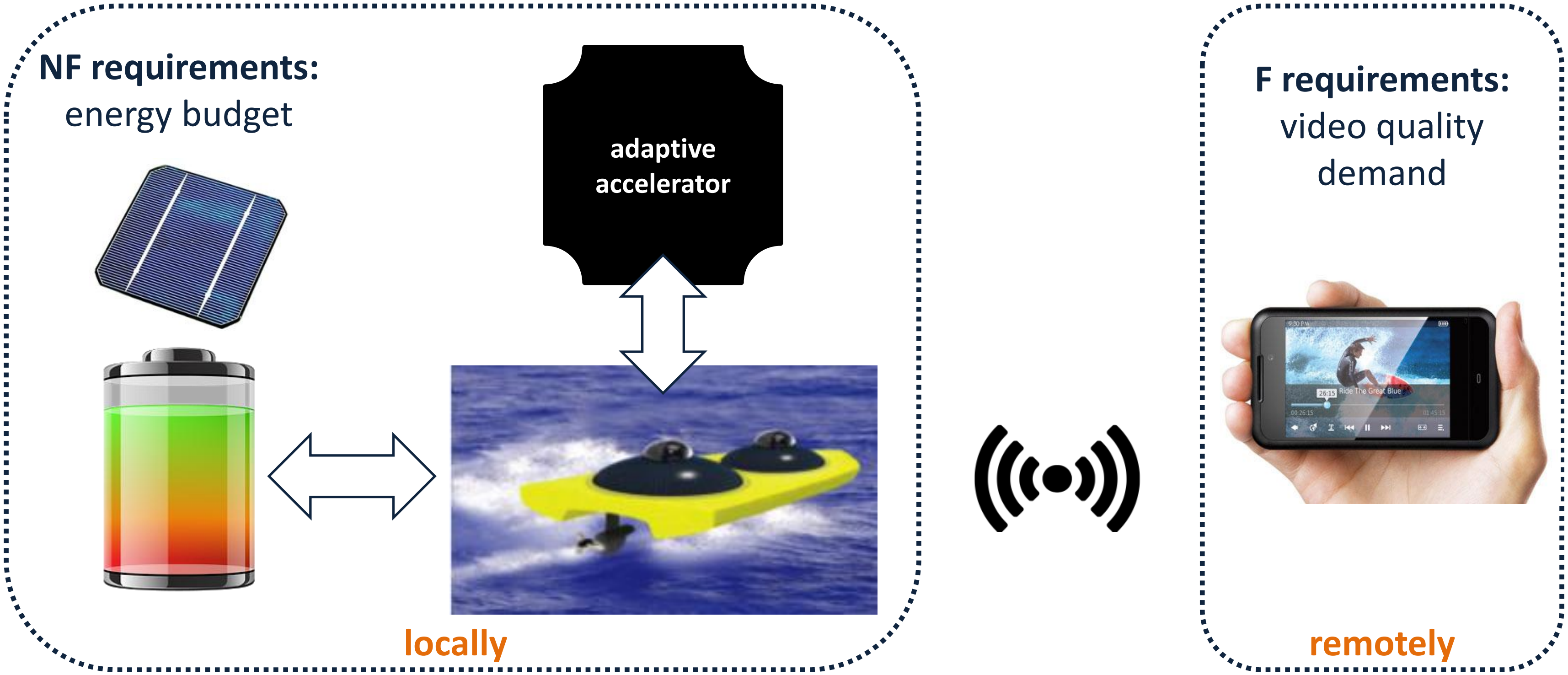
- Introduction
  - CERBERO and Cyber Physical Systems
  - HEVC Codec and Software Approximate Computing
- Approximate HEVC interpolators
  - Coarse-Grained Reconfiguration
  - From CG HEVC Interpolators to CGR HEVC Interpolators
- Results
  - Achieved Adaptivity
  - Comparison with the State of the Art
- Conclusions

Conclusions

- **CERBERO**: continuous design environment for **Cyber-Physical Systems** (CPS)
  - run-time F/NF requirements driven adaptivity
- **HEVC** power/energy hungry, latest video coding standard
  - **Approximate computing** on HEVC interpolators demonstrated to provide energy versus quality trade-off
- **Coarse-Grained Reconfiguration** (CGR) allows approximation of HEVC interpolators in hardware
  - our solution challenges outperforms state of the art solutions

Future Directions

At the CPS physical level **application specific efficient accelerators** capable of providing **flexibility and dynamic adaptation to changeable F/NF requirements**.



Acknowledgements

The CERBERO project has received funding from the EU Commission's H2020 Programme under grant agreement No 732105.

2nd Italian Workshop on Embedded Systems
IWES 2017

Dynamic Trade-Off Management for CPS

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7-8 September 2017 – Rome (IT)