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HEPSYCODE-RTMC: Real-Time and Mixed Criticality Extensions for a System-Level HW/SW Co-Design Methodology

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The growing complexity of nowadays embedded digital systems, especially if based on modern *System-on-Chip* (SoC) adopting explicit heterogeneous parallel architectures, and their reduced time-to-market has radically changed the common design methodologies. Traditional design techniques, based on independent design of HW/SW components are no longer sufficient to support the integration of subparts of such SoCs. Here, HW/SW co-design methodologies, where designers can easily check system-level constraints satisfaction and evaluate cost/performance trade-off for different architectural solutions, are of renovated relevance. Furthermore, a growing trend in embedded systems domain is the development of mixed-criticality systems where multiple embedded applications with different levels of criticality are executed on a shared hardware platform (i.e. mixed-criticality embedded systems). The criticality of an application is an indication of the level of integrity and/or persistence required for the application itself. The main problem in the management of a mixed criticality system is to ensure that low criticality applications do not interfere with the high criticality ones. This type of systems can be found in many domains such as aeronautics, aerospace, and automotive industry, where applications are always characterized by the presence of tasks whose execution is critical (typically related to safety issues) and tasks whose execution is not critical. For example, high critical control functions, like the ones related to the navigation control system, can coexist with the less critical ones related to the entertainment system. The two categories (i.e. critical and non-critical) can be further divided by identifying different criticality classes. The goal is always to allow these applications to interact and coexist on the same platform, but a proper management of such mixed criticality systems becomes a very complex task that poses also several challenges from the implementation point of view.

In such a scenario, this presentation focuses on a framework (and related tool) for modeling, analysis and validation of mixed critical systems, through the exploitation of an existing "Model-Based Electronic System Level (ESL) HW/SW Co-Design" methodology, improved to provide estimates, metrics and simulations able to consider both real-time (RT) and mixed-criticality (MC) requirements. Starting from different HW-based, OS-based, and Hypervisor-based solutions (both in the research and industrial domains), we provide a classification of different works in the mixed criticality system scenarios, to help both researchers and industries to find resources as close as possible to their needs. Next, we presents a HW/SW co-simulator to be integrated into an ESL HW/SW co-design methodology targeting embedded heterogeneous parallel systems with MC and RT constrains. Hopefully, the final result will be a methodology able to support mixed-criticality systems developments by suggesting both the platform and mapping solutions for the specific mixed-criticality application.

References

[1] Ciambrone, D., V., Muttillo, V., Valente, G., F., Pomante, L.: "HW/SW Co-Simulator for Embedded Heterogeneous Parallel Systems", In: Euromicro Conference on Digital Systems Design (DSD 2017) - Work in Progress Session, Vienna, Austria, Aug. 30 - Sep. 1, 2017

[2] Muttillo, V., Valente, G., Pomante, L., Tiberti, W.: "HEPSYCODE-RT: a Real-Time and Mixed Criticality Extension for a System-Level HW/SW Co-Design Methodology", In: 2017 International Conference on High Performance and Embedded Architecture and Compilation (HiPEAC), Stockholm, Sweden, 23-25 Jan. 2017

[3] Federici, F., Muttillo, V., Pomante, L., Serri, P., Valente, G.: "A Model-Based ESL HW/SW Co-Design Framework for Mixed-Criticality Systems", In: EMC² Summit at CPS Week, Vienna, Austria, 11 April 2016

[4] Muttillo, V.: "A Survey of Mixed-Criticality System Implementation Techniques", In: EMC2 at Mixed-Criticality Systems Workshop (MCC), Barcelona, Spain, 22 Nov. 2016

[5] Muttillo, V.: "An integrated ESL methodology for developing embedded parallel systems in mixed-criticality scenarios", In: Italian Workshop on Embedded Systems (IWES), Pisa, Italy, 19-20 Sept. 2016