Università degli Studi di Cagliari
EOLAB
Microelectronics and bioengineering lab

Paolo Meloni

Paolo.meloni@diee.unica.it

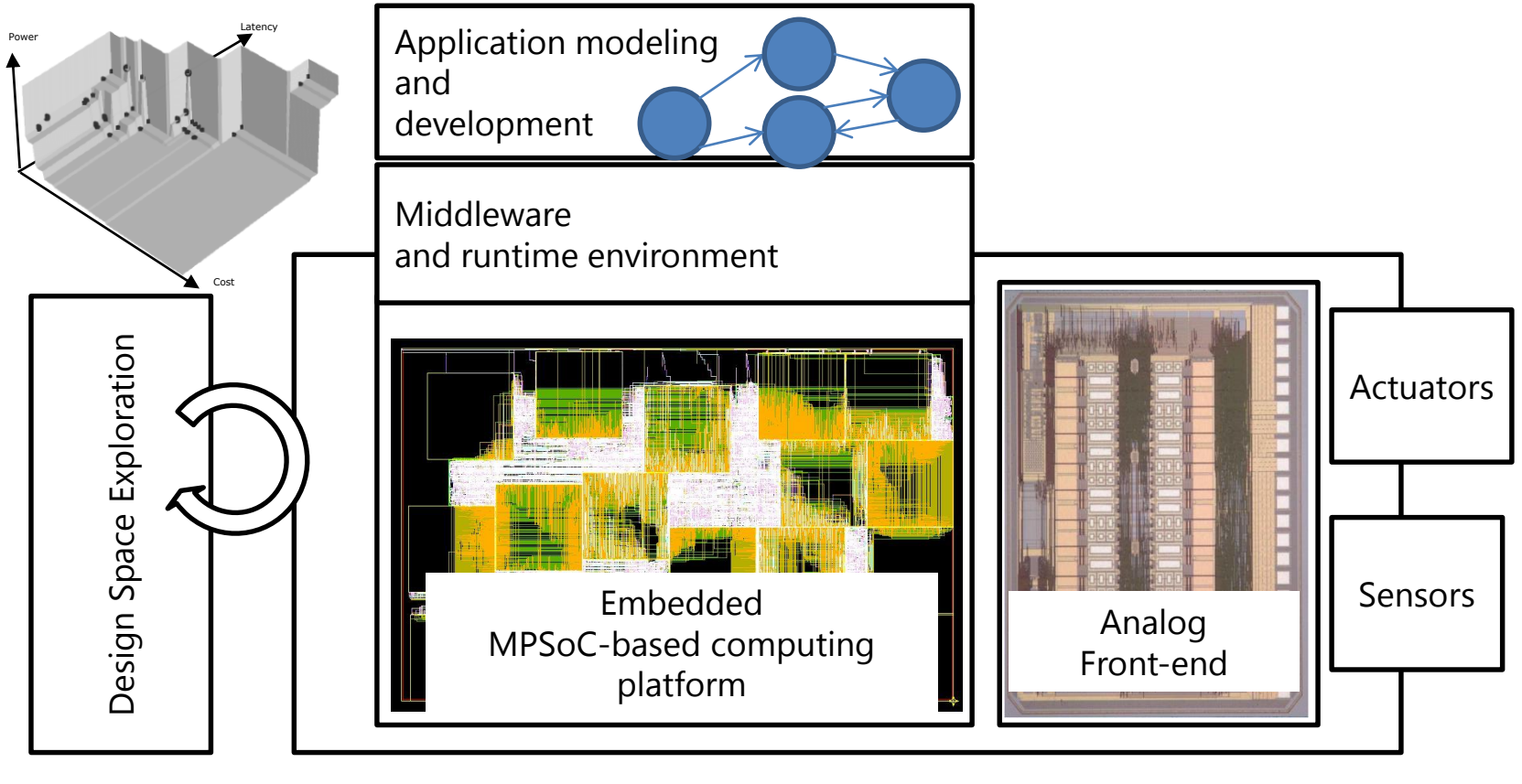
STAFF @ EOLAB

- 1 Full professor
- 1 Associate professor
- 2 Assistant professors
- 5 Post-doc researchers
- 8 PhD students and scholars

- Teaching activities
  - Base electronics courses (Digital and analog design)
  - ARCHITETTURE DI PROCESSORI E SISTEMI INTEGRATI
    - ARCHITETTURE DI PROCESSORI (5 CFU)
    - SISTEMI EMBEDDED (5 CFU)
  - Master in embedded systems for IoT

Embedded systems @ EOLAB

- Tools and methodologies for embedded system design
- Innovative application-specific cisrcuits and systems
- Programming and runtime management of (parallel) embedded systems



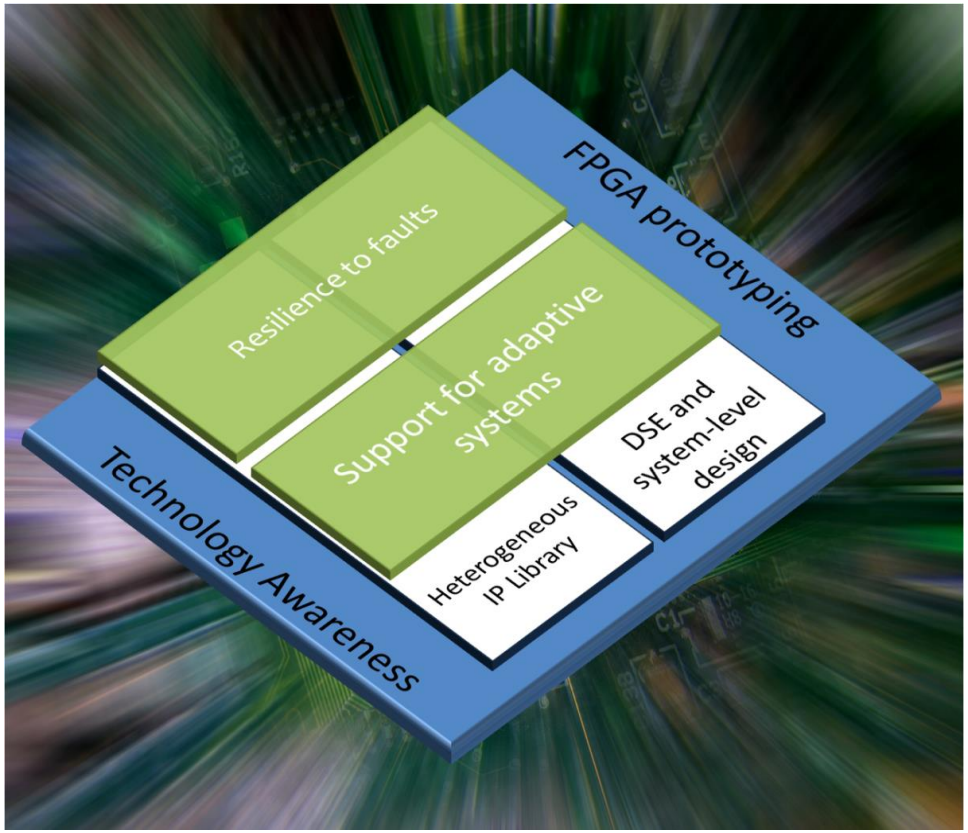
MADNESS - ASAM project

Main goal: define innovative methodologies for system-level design,

optimal composition of embedded MPSoC architectures, according to the requirements and the features of a given target application field.

New challenges, related to both architecture and design methodologies, arising with the technology scaling, the need for system reliability and the ever-growing computational requirements of modern applications.
The proposed methodologies will extend the classic concept of design space exploration to:

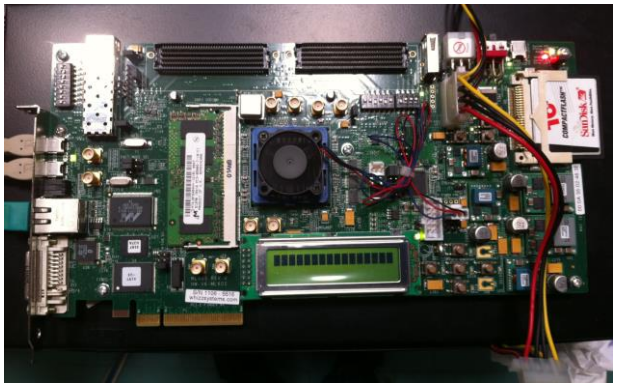
- Improve design predictability, to bridge the *implementation gap*
- Consider fault resilience as one of the optimization factors to be satisfied
- Support adaptive runtime management of the architecture

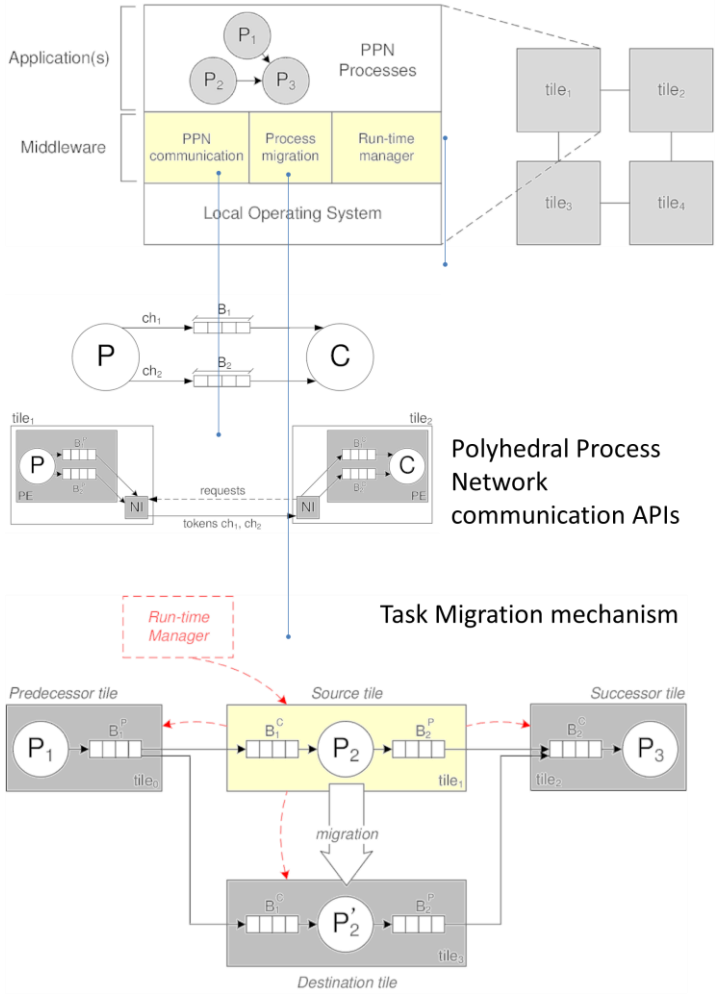


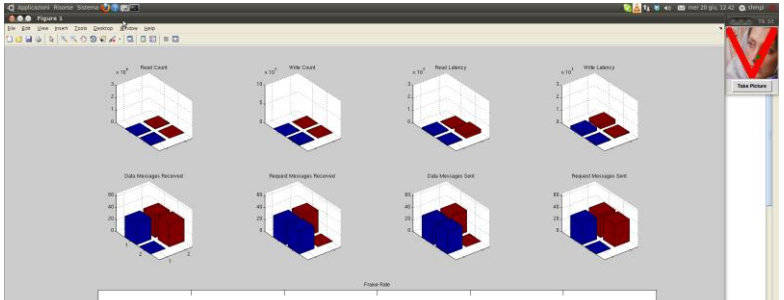
Paolo Meloni, PhD - paolo.meloni@diee.unica.it

MADNESS - ASAM project

- Application-driven customization of mapping of SW tasks on MPSoCs
- Customizing macro- and micro-architectural customization
- Fault-tolerance and adaptivity through task migration
- FPGA-based prototyping
- www.madnessproject.org
- www.asam-project.org







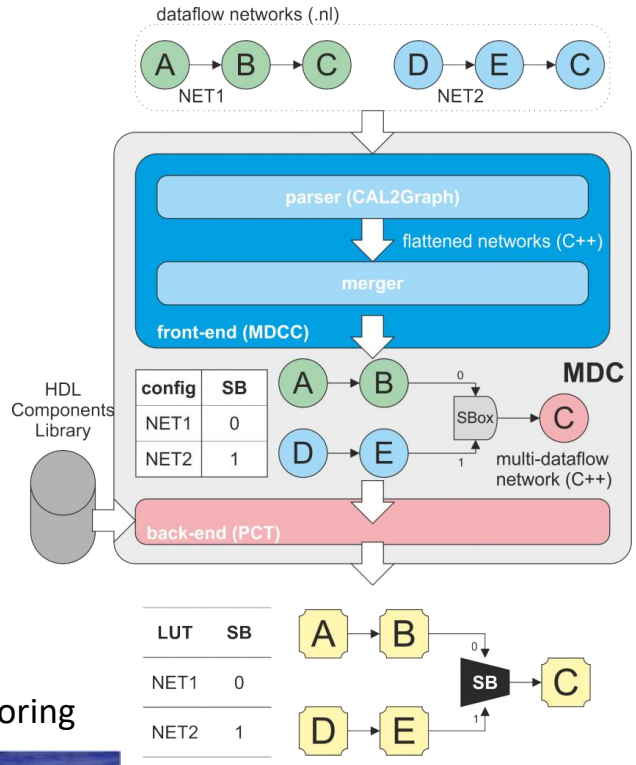
CERBERO project

Cross-layer modEl-based framewoRk for multi-oBjective dEsign of Reconfigurable systems in unceRtain hybRid envirOnments

http://www.cerbero-h2020.eu/

Continuous design environment for Cyber-Physical Systems (CPS) including modelling, deployment and verification

UNICA's task: Reconfiguration of dataflow-based hardware accelerators



Self-healing system for planetary exploration

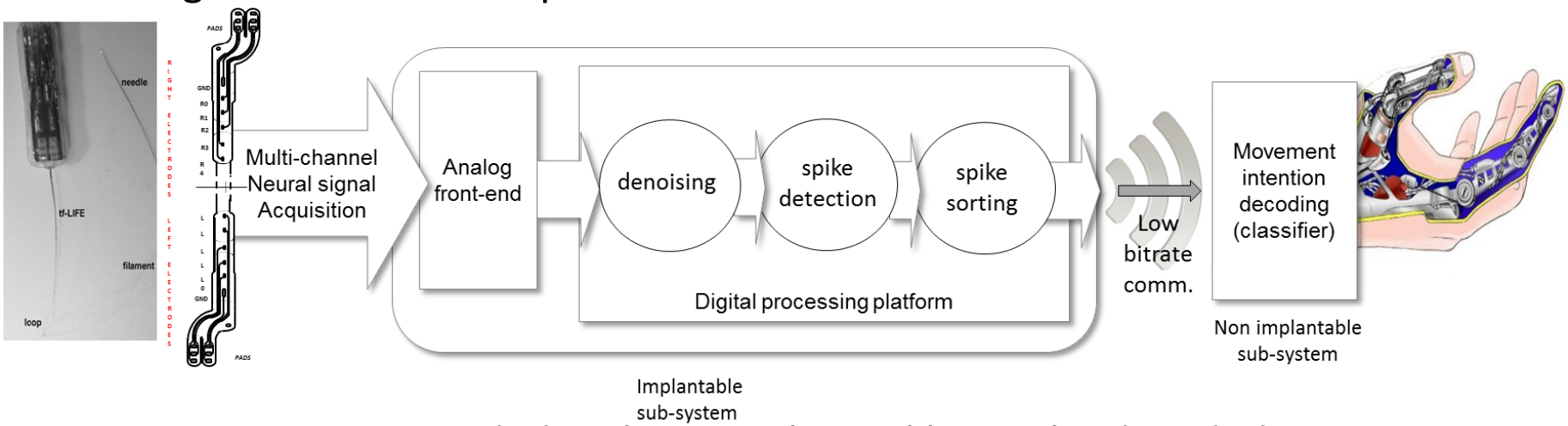
Smart Travelling for Electric Vehicle

Oceans Monitoring

Paolo Meloni, PhD - paolo.meloni@diee.unica.it

NEBIAS- ELoRA project

- Sensing of PNS to control prosthetic device



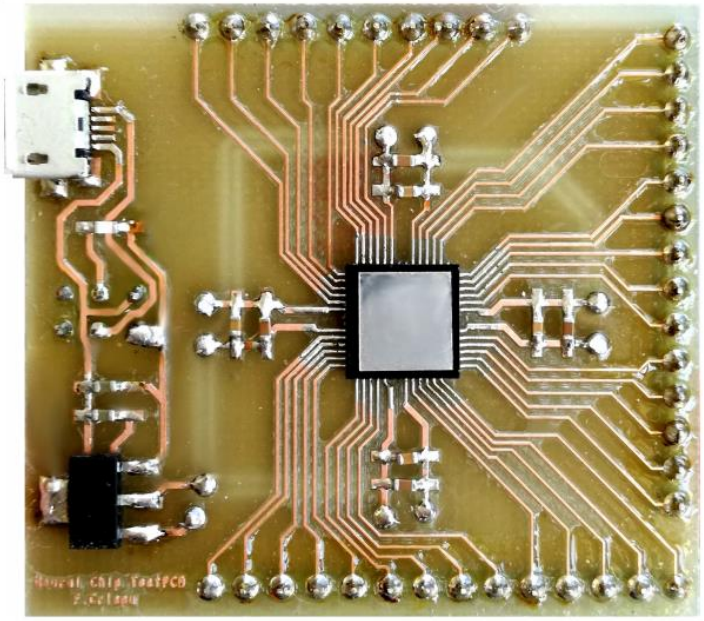
- Motion intention encoded in the neural signal has to be decoded to implement the control loop (neural spike sorting)

http://www.nebias-project.eu/

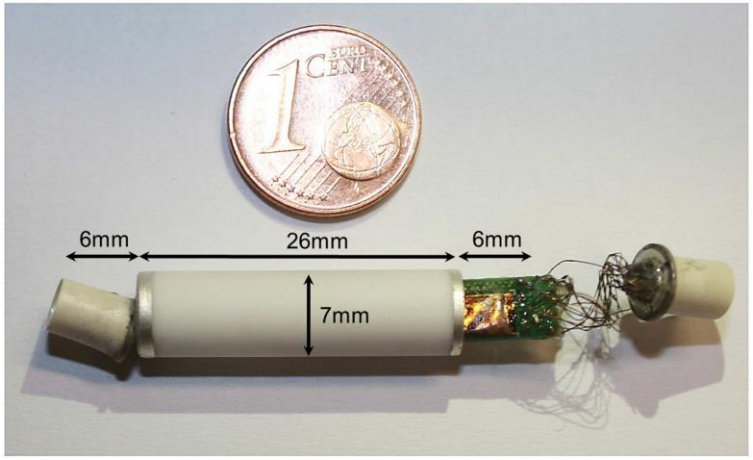
Recorded at EOLAB
Courtesy of Prensilia s.r.l.

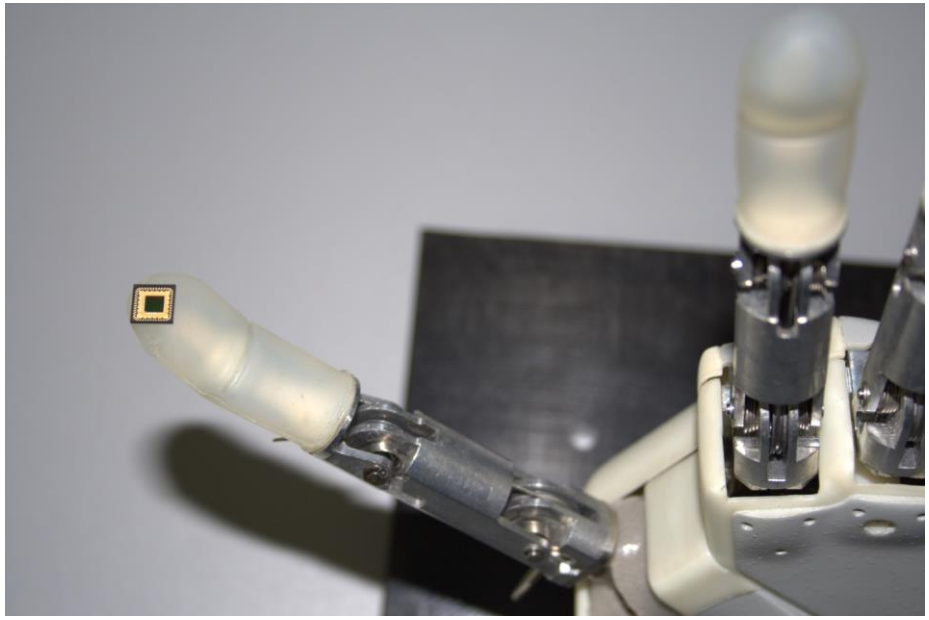
NEBIAS- ELoRA project

- Test chip implemented on TSMC 65nm



CHIP Architecture: 1 GP processor + 2 ASIP
Clock frequency:180 MHz
Power consumption: around 20 mW for maximum neural activity
More than 24 hour before recharging implantable batteries



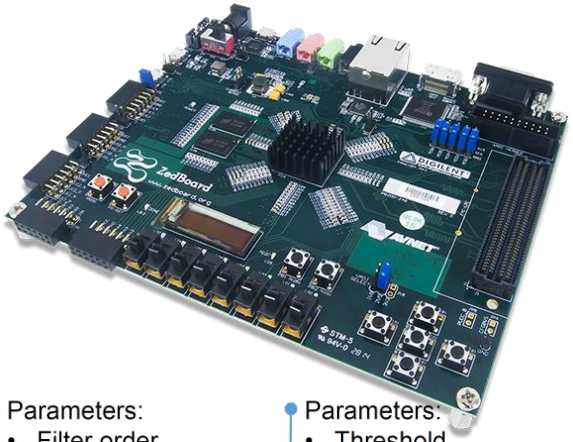


HEADSHIP project

Closed-loop analysis of biological signals acquired by High-density Micro-Electrode Arrays

Data

Stimuli



Data

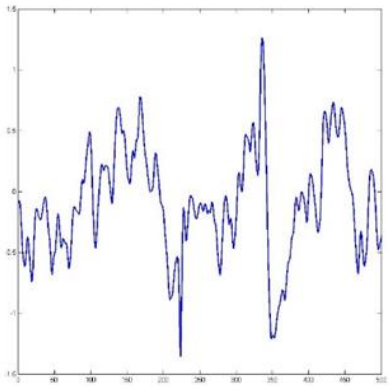
Parameters:
- #input channels
- Sampling frequency

Parameters:
- Filter order

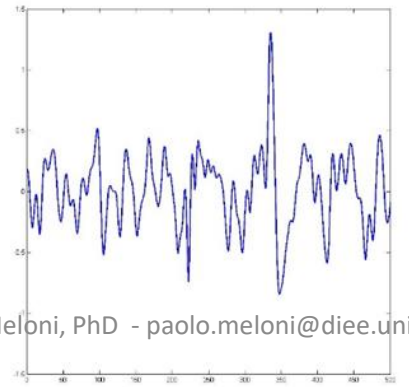
Parameters:
- Threshold generation frequency

Parameters:
- I/O bandwidth

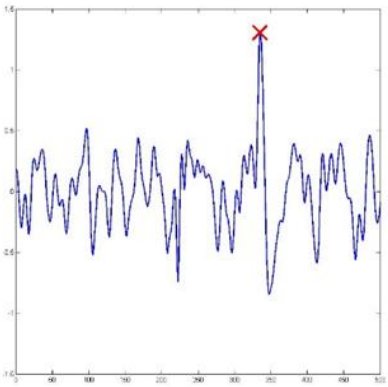
Acquisition front-end → BPF → Spike detection → Sample storage → Processing and storage sub-system



BPF

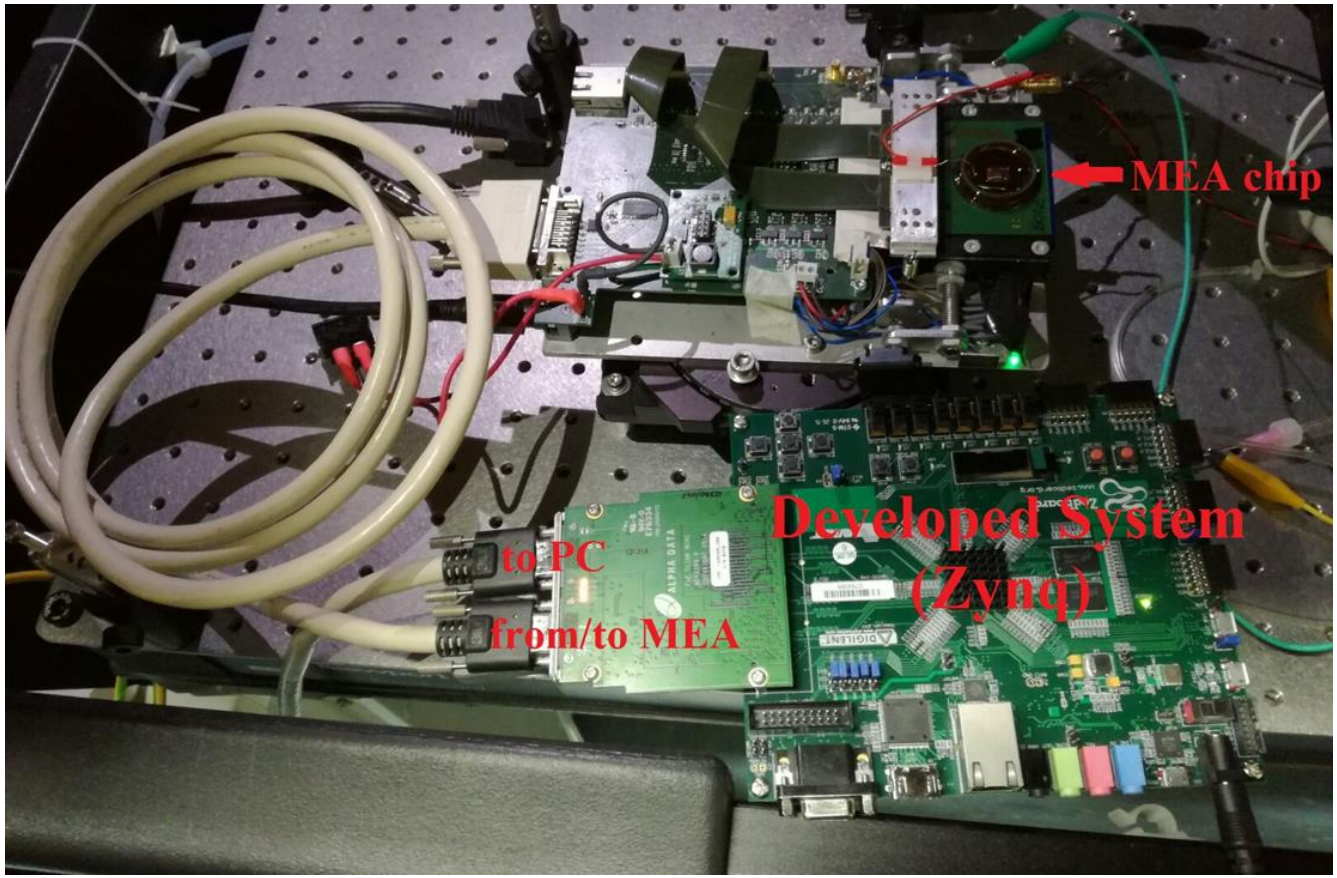


Spike Detection



Paolo Meloni, PhD - paolo.meloni@diee.unica.it

HEADSHIP project



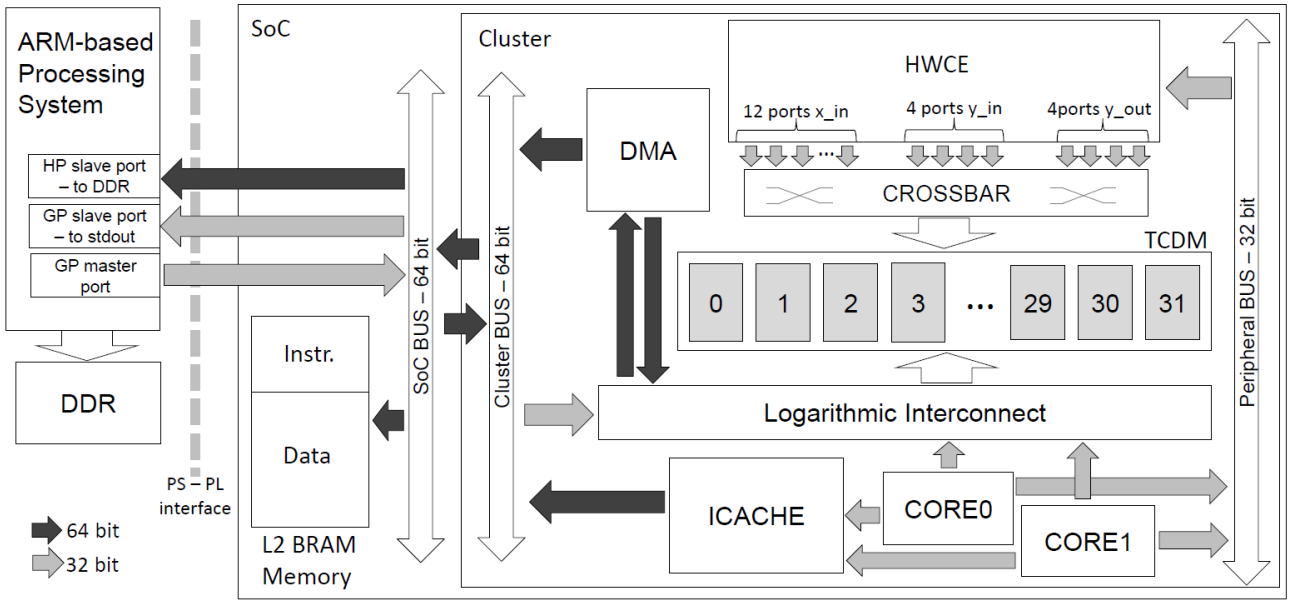
Functional prototype:

- 2.65 GMAC/sec on a Zed board
- Close-loop latency < 2ms
- parallel processing of 4096 channels

NEURAGHE project

Accelerate video-image recognition using FPGAs

- Deep Convolutional Neural Networks accelerator
- Mixed (ARM + Programmable logic) solution
- Performance: 129 GMAC/s
- Clock Frequency: 150 MHz
- Power consumption<10W



paolo.meloni@diee.unica.it

Thank you!

Paolo Meloni, PhD -
paolo.meloni@diee.unica.it