# Efficient FPGA implementation of a Digital Transparent Satellite Processor

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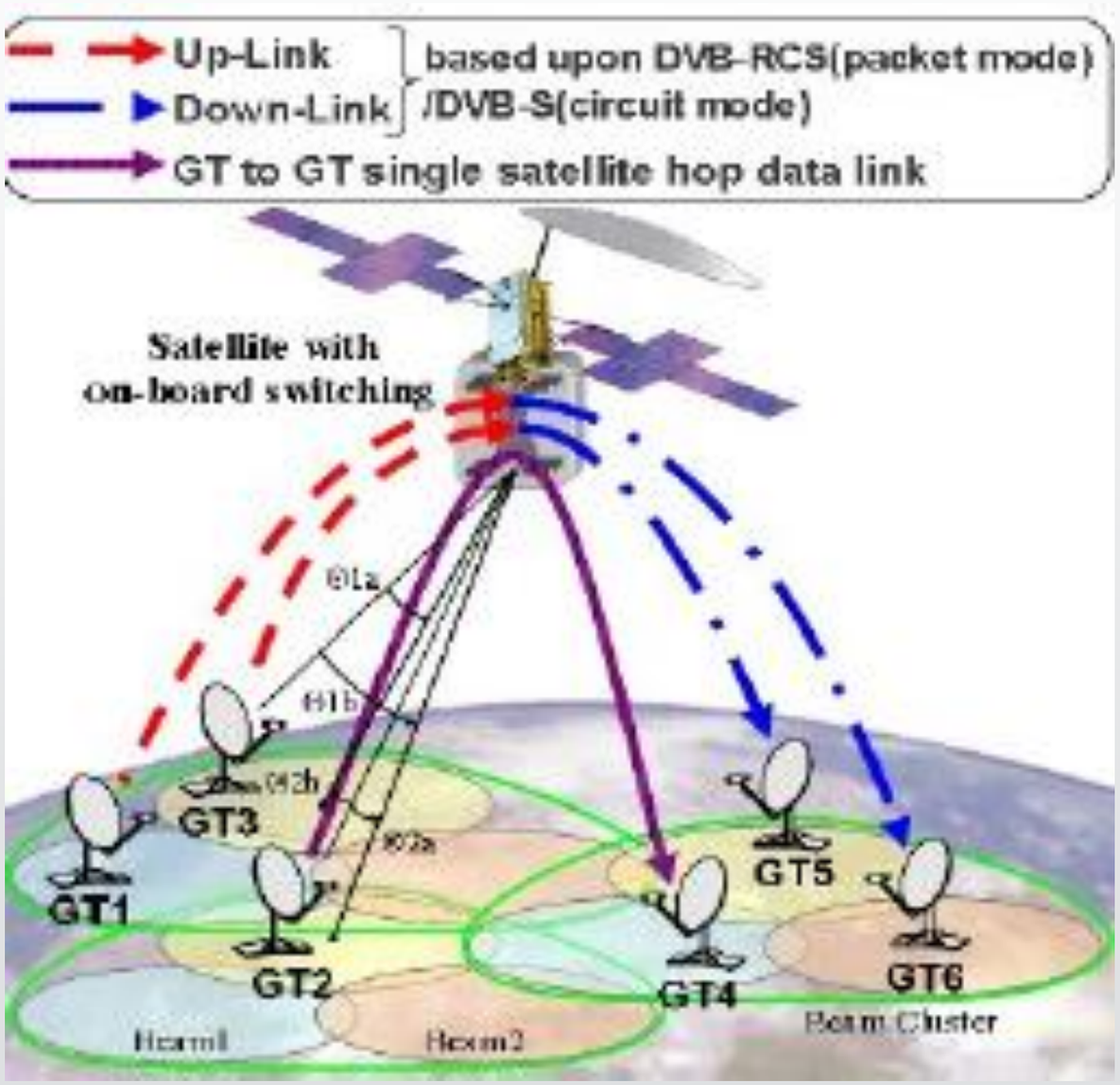
# Outline

- Introduction
- Problem Definition
- Resolution Method
- FPGA Implementation
- Results
- Conclusion
- Future Work

# Introduction(1)

In **satellite** systems for **telecommunications** a great deal of interest concerns the **mesh topology**




**[Mesh topology]**

# Introduction(2)

**Four alternatives for the architecture of a satellite transponder**:

- Fully transparent payload
- Fully regenerative payload
- Digital transparent payload
- Digital Semi-transparent payload

# Introduction(3)

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**Digital Transparent Processor (DTP) is involved**

# Introduction(4)

**Four alternatives for the architecture of a satell ite transponder**:

- Fully transparent payload
- Digital transparent payload
- Digital Semi-transparent payload

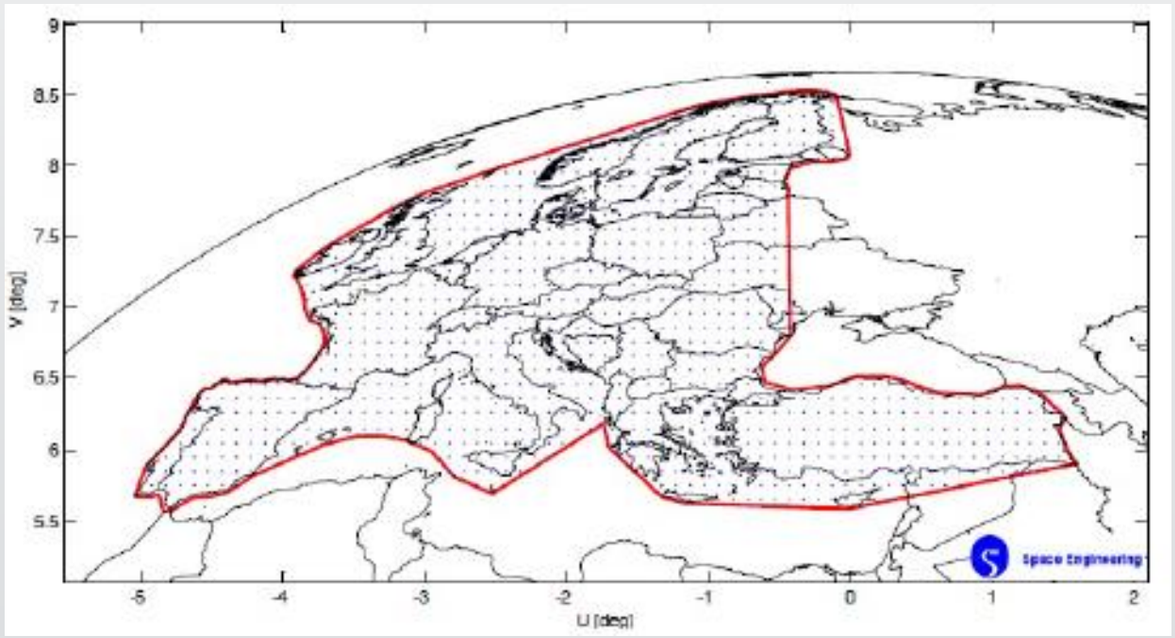
**Digital Transparent Processor (DTP) is involved**

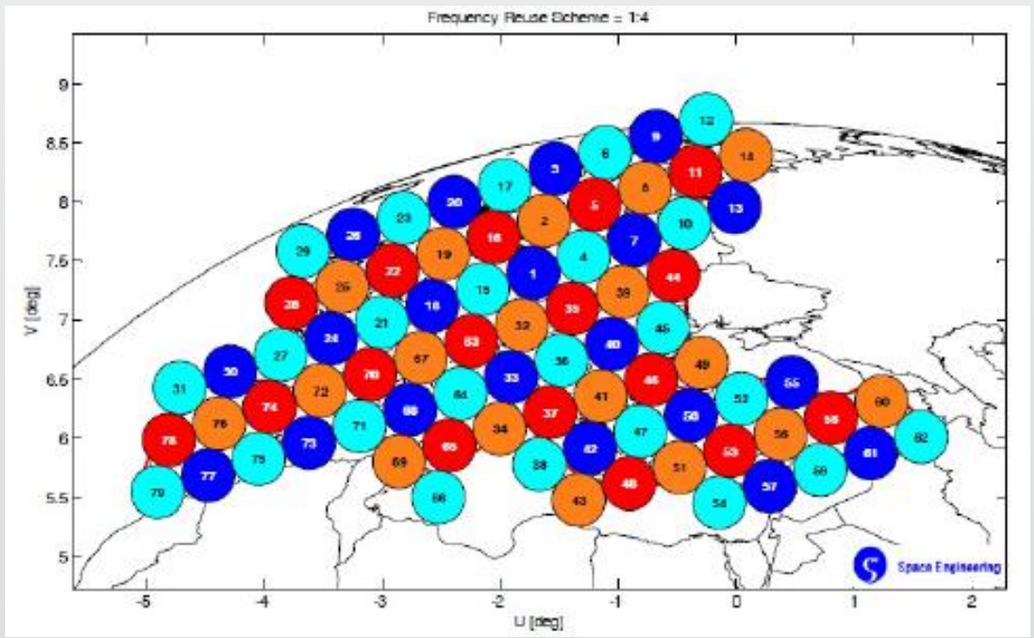
- Support of mesh networking
- Flexibility in the routing
- Frequency planning flexibility

# Introduction(5)

**Scenario of interest:**

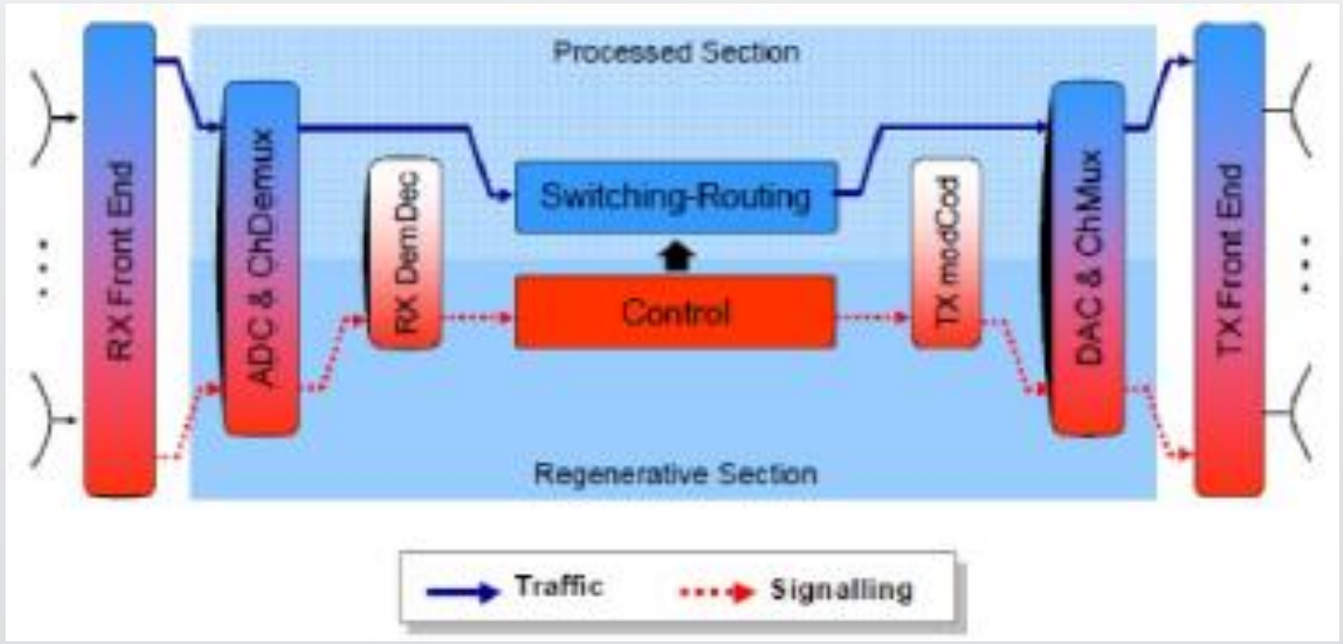
- 79 beams (with 125 MHz allocated per beam) with fully connectivity and flexible routing in frequency, time spatial domains



# Introduction(6)

In this context the digital **semi-transparent payloads** have been recently devised and investigated



# Problem Definition(1)

- A digital transparent/semi-transparent satellite payload can be see as a **hybrid analog-digital on-board chain**

- Modelling and design approaches have so far almost missed the ability to capture in an adequate way these important features

# Problem Definition(2)

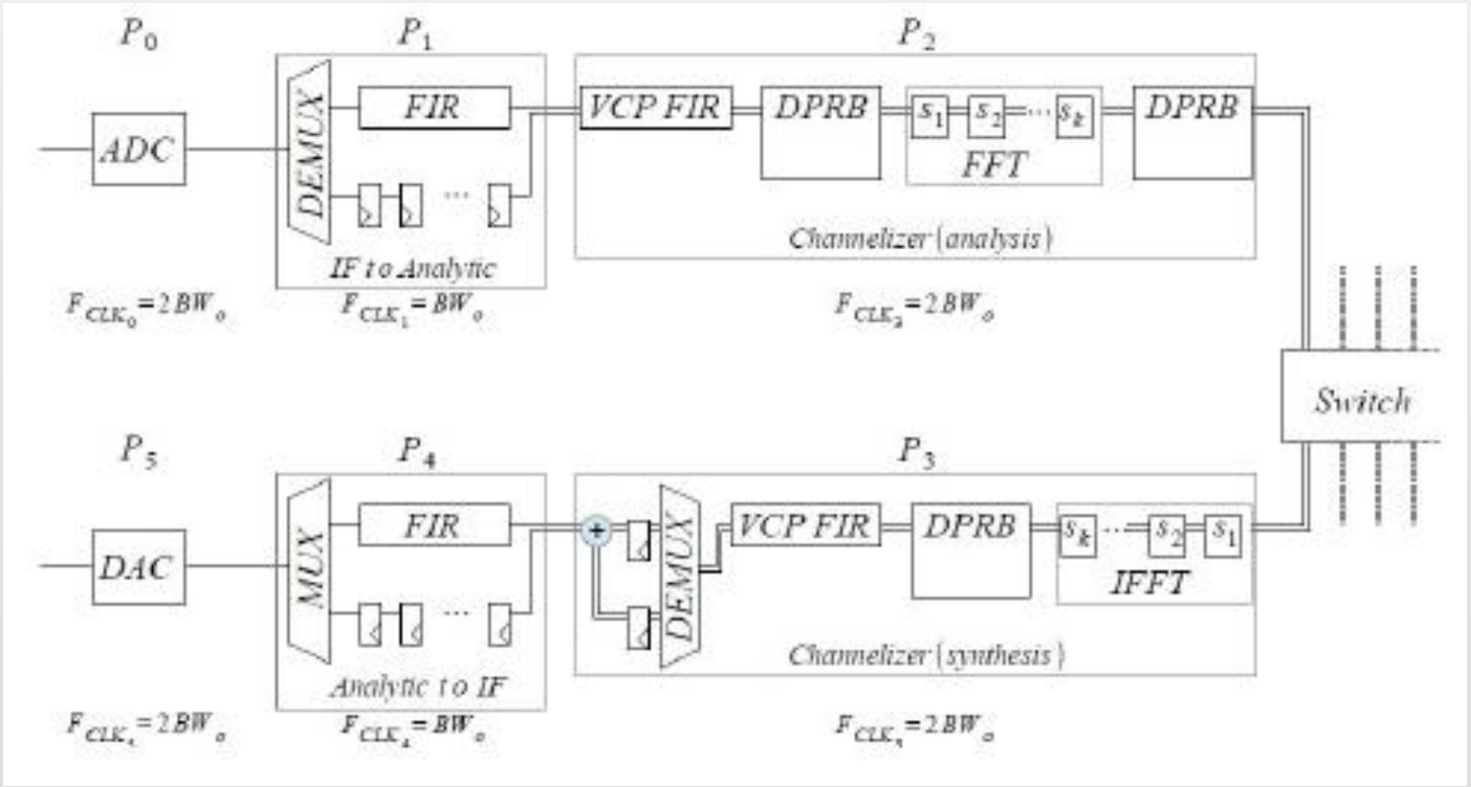
Problem:

**To provide a method that, given the link-budget requirement, provides a detailed definition of digital HW components in the DTP**

# Resolution Method(1)

**Step 1**:

- Define a System Model of DTP-based Transponder




A DTP processing chain is composed by:

- $P_0$: ADC
- $P_1$: Analytical signal extrapolation
- $P_2$: Channalizer (analysis)
- Switching
- $P_3$: Channalizer (synthesis)
- $P_4$: IF signal extrapolation
- $P_5$: DAC

# Resolution Method(2)

**Step 2**:

- Develop an equivalet noise model for the whole DTP chain to understand how link level performance (the DTP noise figure) may impact on the DTP hardware complexity

# Resolution Method(3)

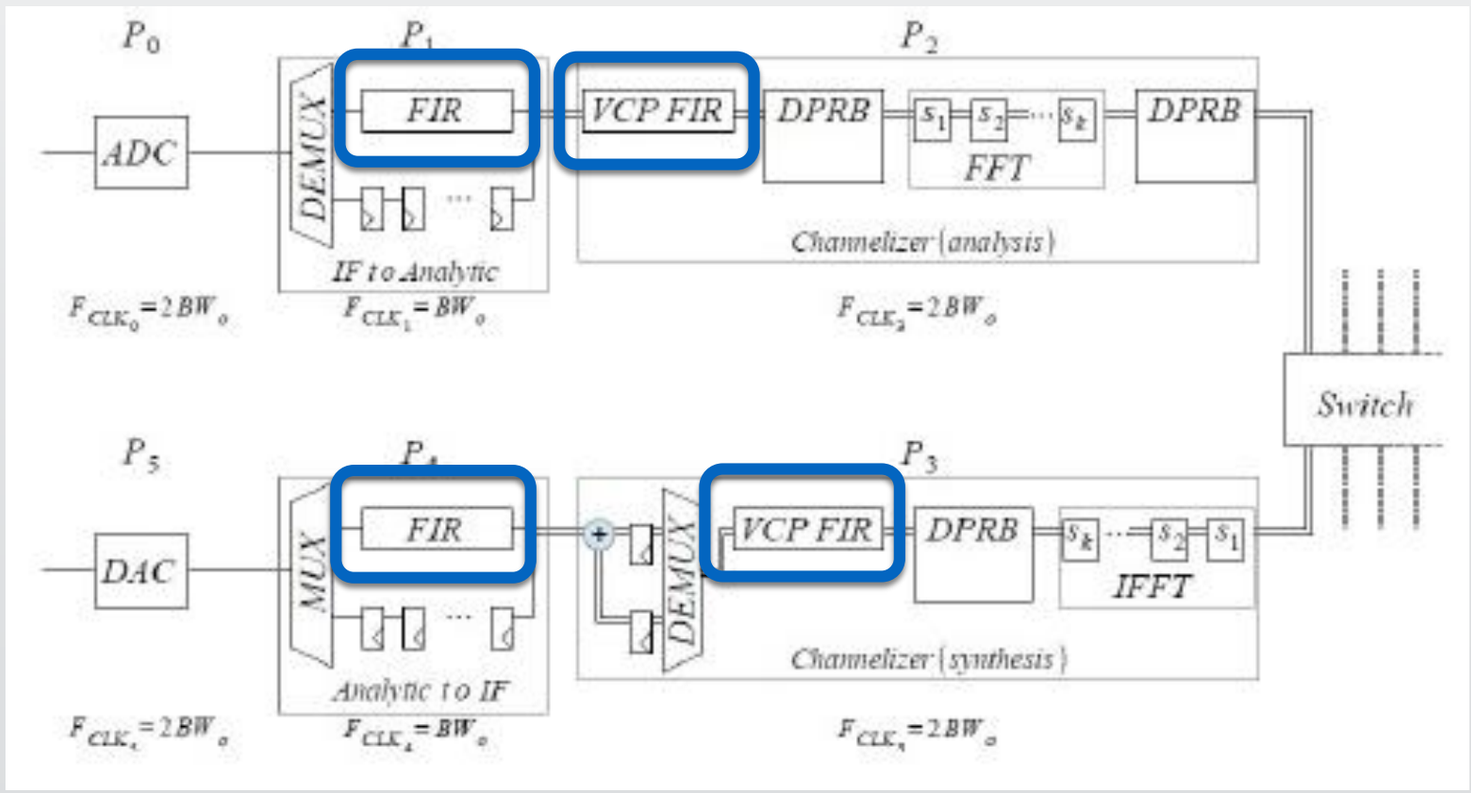
**Step 3**:

- Computing the hardware complexity in terms of:
  i. Number of 2-words multipliers
  ii. Number of 2-words adders
  iii. Number of Flip-Flops
  iv. Number of ROM bits

# FPGA Implementation(1)

The DTP is composed by three basic blocks:

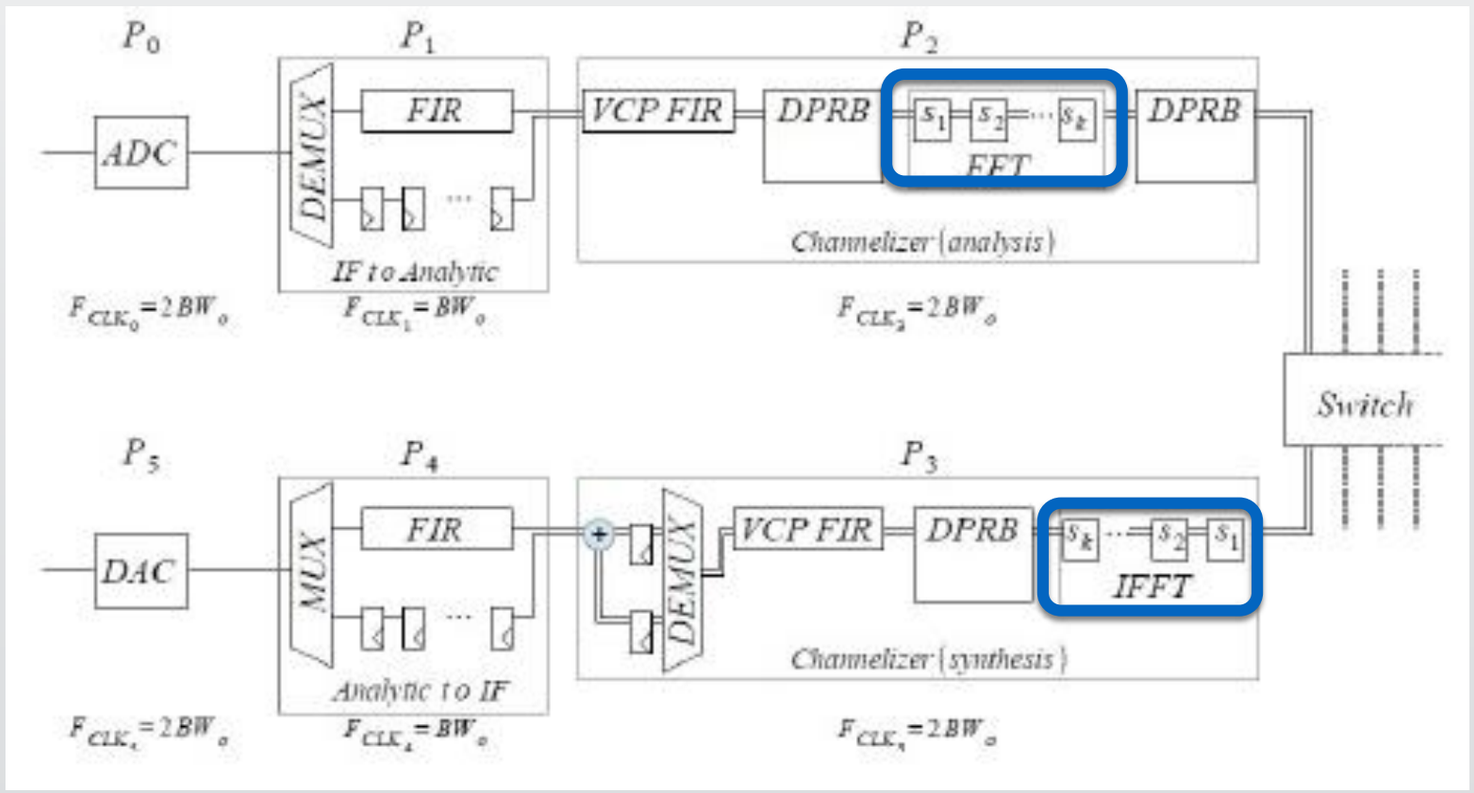
- **FIR** filter elements, implemented in direct form



# FPGA Implementation(2)

The DTP is composed by three basic blocks:

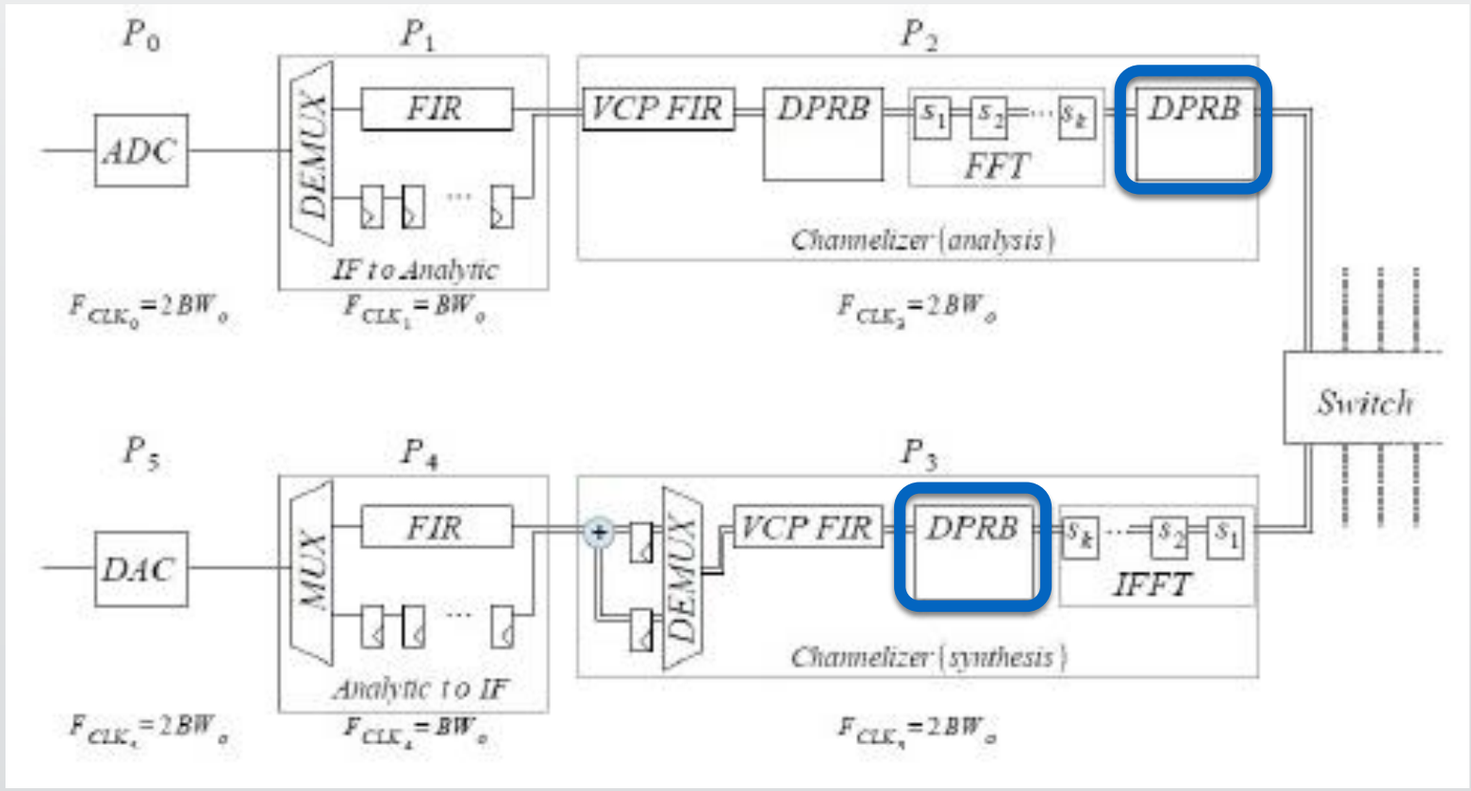
- **FIR** filter elements, implemented in direct form
- **FFT/IFFT** butterfly structures



# FPGA Implementation(3)

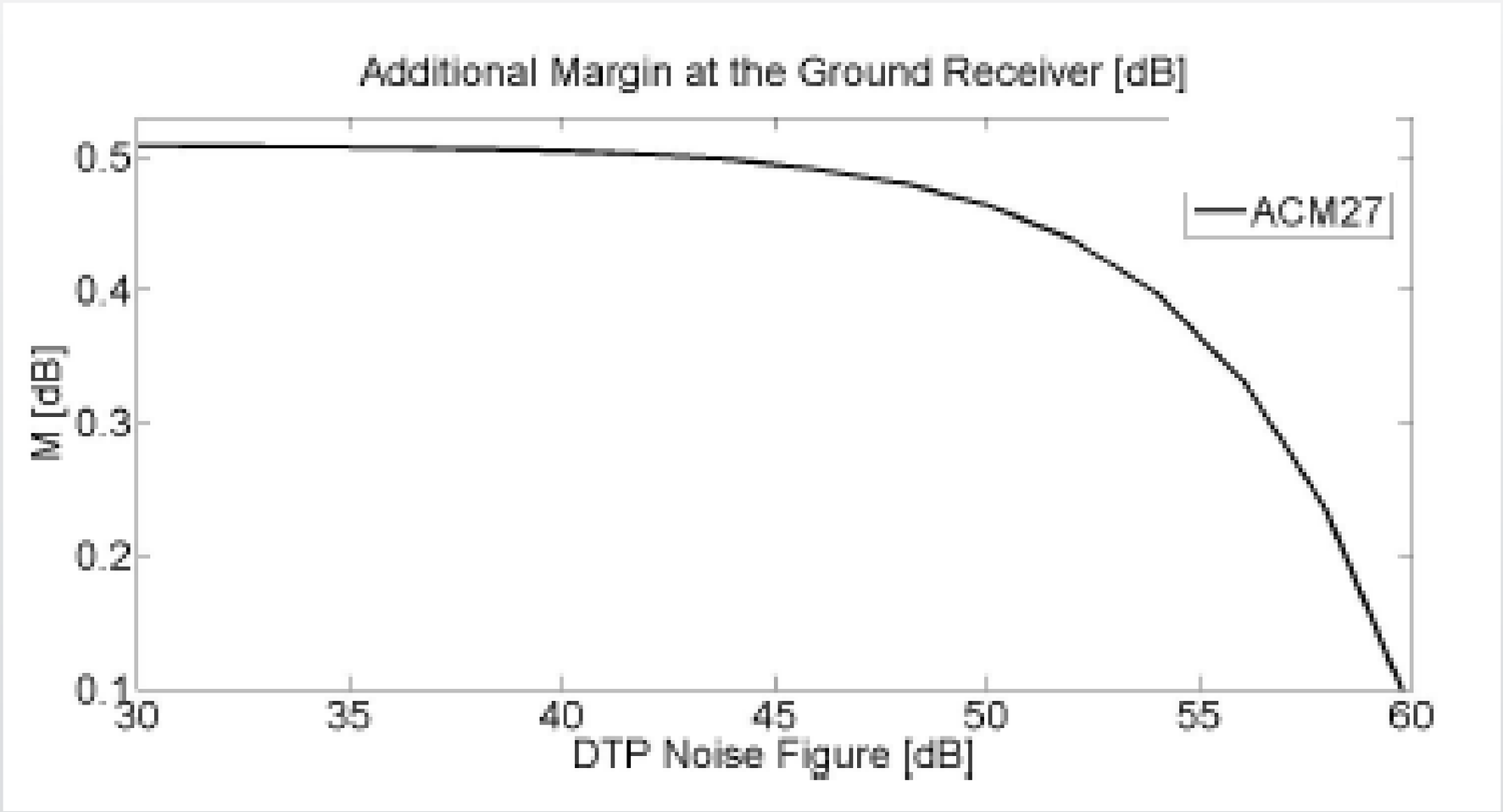
The DTP is composed by three basic blocks:

- **FIR** filter elements, implemented in direct form
- **FFT/IFFT** butterfly structures
- **RAM** buffers



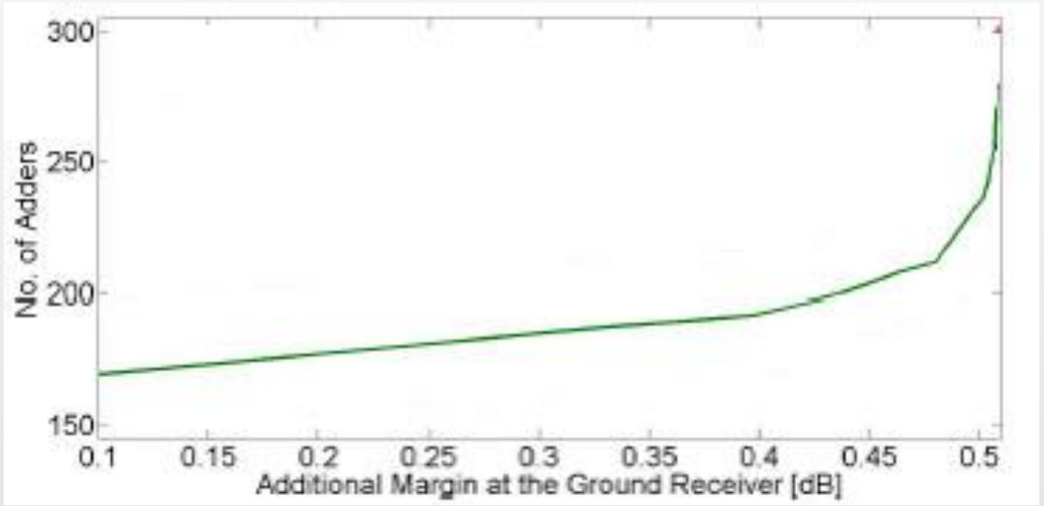
# Results(1)

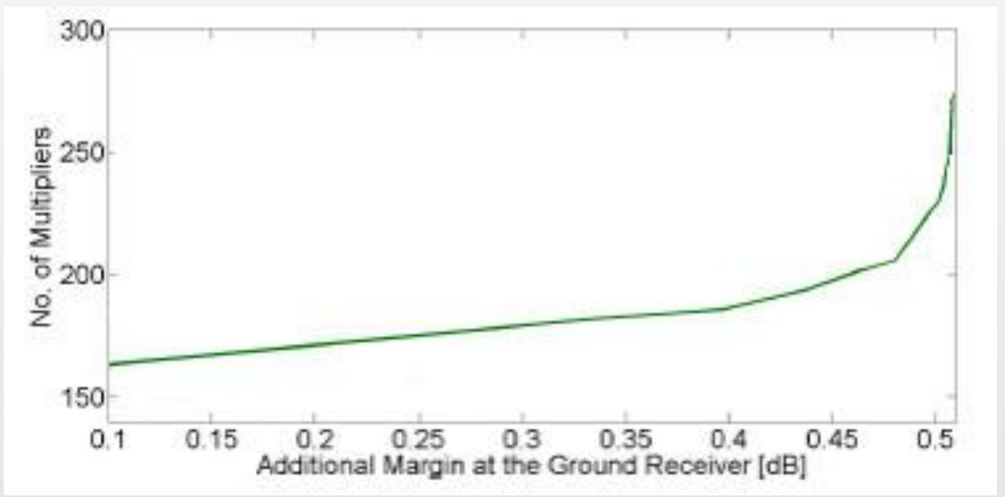
To the increase of DTP Noise Figure corresponds a degradation in the link performance show as reduction in the Additional Margin at the ground receiver

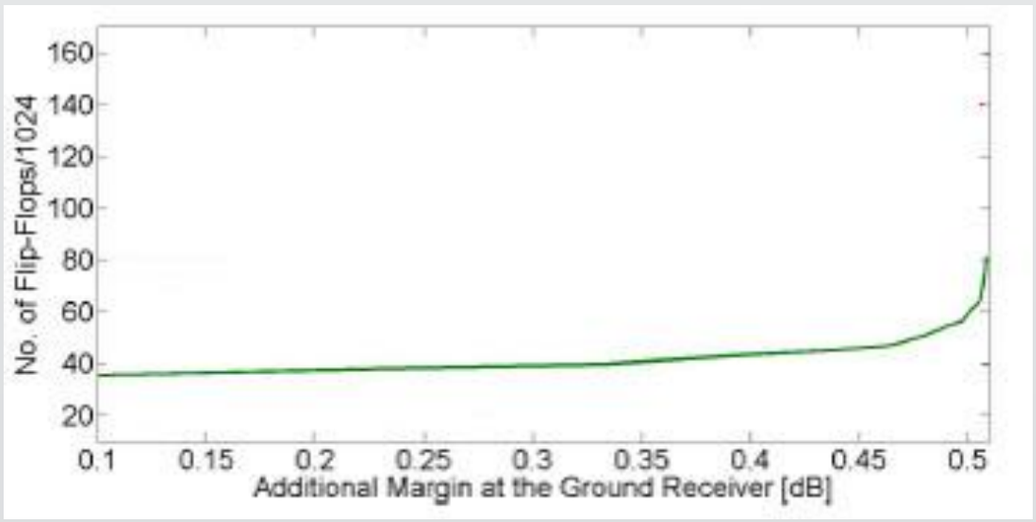


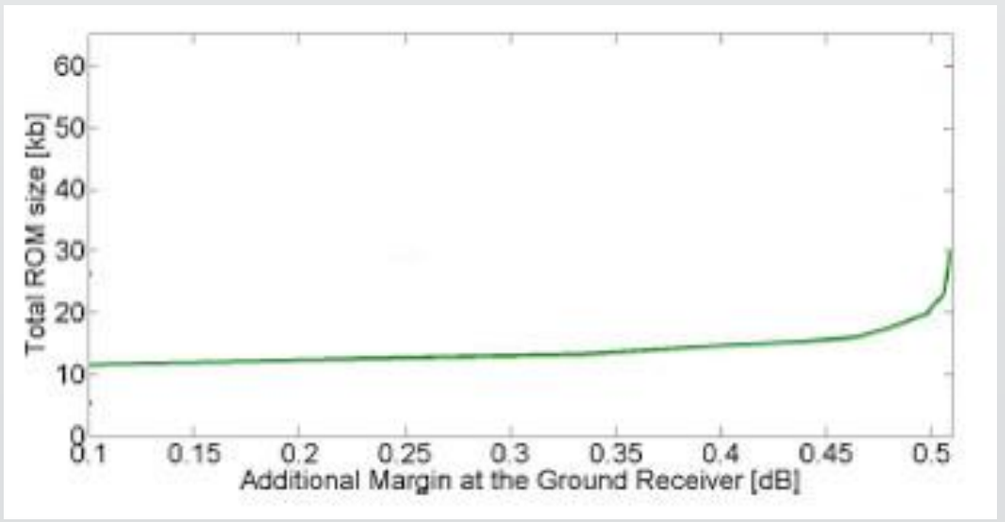
# Results(2)

The DTP Hardware complexity may be directly linked to the chosen working point



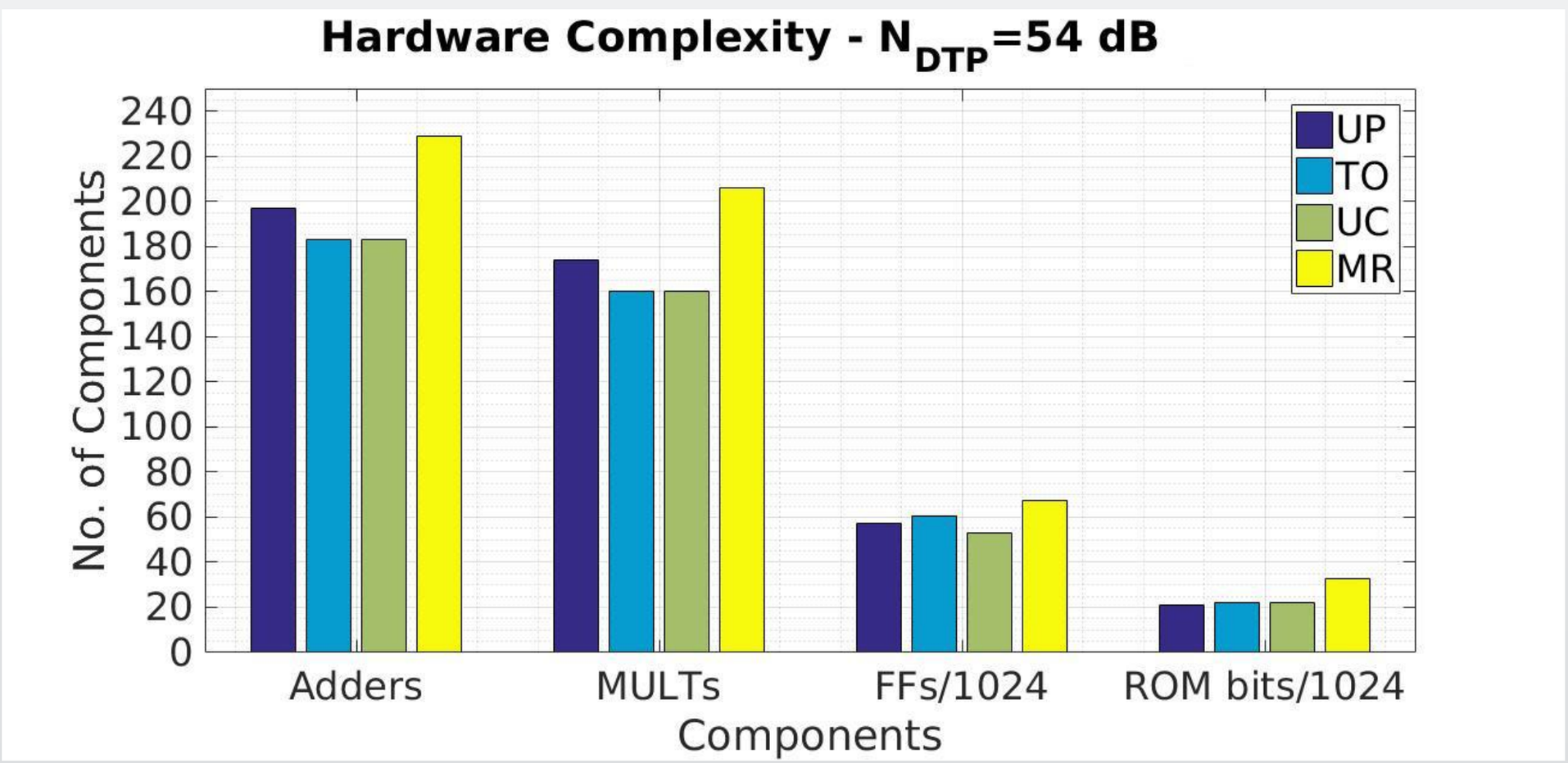



# Results(3)

For a given DTP Noise Figure, different hard-ware complexity can be obtained by applying different design approaches, e.g.:

- UP: Uniform Parameters
- TO: Trade-Off
- UC: Uniform Contributions
- MR: Minimum RAM



# Conclusion

- We have developed a comprehensive framework for **hardware complexity evaluation of novel satellite payloads that rely on semi-transparent transponder architectures**

- The DTP complexity has been related to the overall processed bandwidth, the selected coding and modulation formats, and performance degradation requirements

# Future Work

- Definition of an optimized criterion for DTP hardware design

- Adaptations of the developed framework to several scenarios of interest in satellite communications

# Thanks