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Efficient FPGA implementation of a Digital Transparent Satellite Processor

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The evolution of satellite systems for telecommunications has been driven for decades by the need to overcome the limitation of network configurations relying on pure star topologies, that are typical of transparent satellite architectures, and to support instead more advanced mesh topologies that are typically enabled by regenerative satellite architectures. Current perspectives for satellite communications are massively envisaging the introduction of a new generation of satellites based on semi-transparent transponder architectures. In this frame, technological constraints related to the development and implementation of novel payloads, that include significant on-board digital processing, call for careful system modeling and accurate digital hardware design in order to enable feasible trade-offs between hardware efficiency and overall link-budget performance.

In the context presented above the design and implementation of digital systems based on a top-down approach makes it difficult to accomplish objectives related to execution time and area size while meeting communication performance requirements across the whole satellite link. A bottom-up approach can be instead proposed once a theoretical framework has been developed and a complete design flow has been proposed for a Digital Transparent Processor (DTP): it moves from system requirements and brings to a detailed definition of digital HW components in the DTP. By relying on our extensive work documented in [1]- [5] in this talk we will present and discuss an FPGA-based prototype benchmark that has been developed in our lab to validate the framework.

References

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