The importance of memory in the next generation of real-time systems

The recent multi-core revolution triggered a series of technological challenges involving a wide spectrum of computing applications. As clock speeds cannot be further increased from last decade's standards, the higher number of transistors made available by modern integration technologies is being exploited by integrating multiple cores on the same chip. This is opening to a series of technological challenges in the real-time and embedded computing market, ranging from the parallelization of existing applications, to the simultaneous elaboration of multiple sensor data, to the need for predictable timing guarantees of applications requiring a prompt interaction with the user/environment.

Unfortunately, it is difficult to provide predictable timing guarantees in a platform where multiple cores may contend for shared resources, the most important undoubtedly being the shared memory banks. In the OPEN-NEXT project [1], we intend to bridge this technological gap, selecting the most suitable and practical scheduling techniques from the recent real-time literature, and implementing them on modern embedded multi-core platforms for the embedded market. To this extent, an exhaustive exploration of the targeted computing platform is paramount to assess its potential in terms of predictable performance, and to derive worst-case analysis that can support and schedulability framework.

We will present a preliminary analysis of three cutting-edge platforms for industrial and automotive systems, namely an NXP iMX6 quad-core and two heterogeneous embedded boards, NVIDIA Tegra X1 and Xilinx Ultrascale. In this presentation, we highlight the possible source of contentions of the shared memory banks, that ultimately might harness the performance and predictability potential of the whole platform, and propose techniques to mitigate them.

[1] OPEN-NEXT - *"Strutture software real-time e open-source per piattaforme embedded industriali di prossima generazione"* - PG/2015/737416 – CUP E32I16000040007. Co-funded by ERDF - European Regione Development Fund 2014/2020